



52 MWSCAS 2009

Cancun, México August 2-5, 2009

GENERAL

PROGRAM



Celebrating 125 Years
of Engineering the Future

WELCOME

From August 2nd to August 5th the IEEE International Midwest Symposium on Circuits and Systems (IEEE-MWSCAS'09), the oldest CAS Society conference is held in Cancun, Mexico, one of the most beautiful resorts of the world, in which the participants attending the MWSCAS2009 and their accompanying persons may enjoy from the wonderful Caribbean Sea beaches, top class shopping centers and restaurants, as well as the famous Kulkulkan Pyramid in the archeological zone of Chichen Itza. Cancun also offers the visitor wonderful and unique aquatic parks such as Xcaret, among many other interesting places that do the visit to Cancun and unforgettable experience.

The organizing committee of the MWSCAS2009, welcomes you to Mexico, in the city of Cancun, from August 2nd to August 5th, 2009. The wide area of topics covered this year which drew an important number of submissions (478) from all over the world. These were categorized and sent to a large number of reviewers carefully selected by the Technical program committee members, who performed the important task of reviewing and selected them. We feel very much indebted to them for their invaluable help to bring the quality level of IEEE-MWSCAS2009 to a high standard to which our scientific community has grown accustomed. Based on those reviews, (290) papers were selected for presentation in lecture or poster sessions.

IEEE-MWSCAS2009 will encompass an important number of tutorial sections and keynote talks given by prominent experts covering key areas of research in the field of Circuit and Systems, that we hope will provide all attendees a unique forum for the exchange of ideas and results. Furthermore, the technical program committee has assembled an excellent program, the result of hard work and dedication by many individuals. We would like to take this opportunity to thank all the members of the organizing committee, the technical program committee, the various speakers, our sponsors, the many reviewers and most of all the authors for contributing their research work.

We also thank to the researchers from all around the world, for choosing to submit their contributions to IEEE-MWSCAS. Due to their important contributions, it was possible to create a technical program of high scientific quality enriched by three plenary talks and technical sessions. We believe that we have met the challenge to provide wonderful environment for our colleagues to discuss the important developments in our work.

We encourage you to enjoy the hospitality of Cancun, its world class shopping centers, restaurants and wonderful archeological places, as well to renew academics relations and do new ones. We hope that you will find IEEE-MWSCAS2009 to be innovative and exciting, that you will all acquire valuable new insights from this academic event.

Prof. Hector Perez-Meana
MWSCAS2009 General Chair

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SUNDAY 2

Registration Desk 8:00-17:00 hrs.

Welcoming Reception 19:00 hrs. **Swimming Pool Area**

Tutorials

	-Room A	Room B	Room C	Room D
10:00 – 11:25	Tutorial. 1	Tutorial. 2	Tutorial. 7	
11:25 – 11:35	Coffee Break	Coffee Break	Coffee Break	
11:35 – 13:00	Tut. 1	Tut. 2	Tut. 7	
15:00 – 16:25	Tutorial. 4	Tutorial. 5	Tutorial. 6	Tutorial. 3
16:25 – 16:35	Coffee Break	Coffee Break	Coffee Break	Coffee Break
16:35 – 18:00	Tut. 4	Tut. 5	Tut. 6	Tut. 3

1. Design of Low voltage power efficient analog and mixed signal circuits in deep sub-micrometer CMOS technology

Jaime Ramirez-Angulo¹, ()*, New Mexico State University, Las Cruces

Various design techniques aimed to obtain low-voltage power-efficient high performance mixed signal circuits are presented. Power efficiency is achieved by employing class-AB stages with high current efficiency based on these techniques. The use of resistive local common-mode feedback and quasi-floating gate transistors is covered in detail. Some applications of the circuits designed using these techniques are included.

(*) In collaboration with:

Ramon G. Carvajal- Escuela Superior de Ingenieros, Universidad de Sevilla, Sevilla, Spain

and Antonio Lopez-Martin, Departamento de Ingeniería Electrónica, Universidad Pública de Navarra, Pamplona, Spain

2. Modern Circuit Techniques and Architectures for Multimedia Receivers

Ahmed A. Youssef, University of Calgary/ Newport Media Inc

Multimedia reception (i.e TV reception) is the latest feature to be added to the handheld device. The broadband nature of the TV band poses many technical challenges in mobile TV receivers design. In this presentation a summary of these design challenges will be presented. New circuit design techniques and architectures will be discussed with an emphasis on approaches that reduce the requirement for off-chip passive filters. Basic concepts related to receiver dynamic range, including noise performance and mechanisms for improving linearity degradation will be introduced. Design approaches that are useful for improving receiver dynamic range, such as feedback and feedforward; the use of on-chip RF passive attenuators and variable gain low noise amplifiers; and approaches that utilize multiple receiver paths will be presented, along with relevant examples from practical mobile TV systems. The presentation will be concluded by proposing some venues of research.

3. A Practical Approach to Switched Capacitor Circuits

David J. Willis, Principal Engineer, ON Semiconductor

Switched-capacitor amplifiers, filters, and data converters offer a good solution to small high accuracy circuits. Text book theory is beneficial in teaching basics about the configurations, noise, etc. The purpose of this tutorial is to go beyond the classroom and expose the student to real life examples and design techniques. The course will be divided into 5 sections. The class will first review the basics of how switched-capacitor circuits work, including integrators, amplifiers and filters. Second, we discuss techniques for reducing $1/f$ noise and offset voltage effects. The third section discusses opamp design criteria for reduced noise and settling. The fourth portion discusses how to determine switch and capacitor sizes for noise and settling. The last section will cover layout techniques for optimal results to get high accuracy circuits. MatLab and SPICE simulation techniques will be included. A review of chapter 10 in Johns and Martin "Analog Integrated Circuit Design" will be helpful before attending the class.

4. BIST and Digital Self-Calibration of Nanometer RFICs

Mohammed Ismail, Professor and Founding Director Analog VLSI Lab, Ohio State University

This tutorial will present design techniques at both the architectural and circuit levels to incorporate built-in-self-test and digital calibration into critical RF blocks, such as LNAs, mixers, VCOs, of complex multi-band CMOS radio transceivers. The ultimate goal is to reduce silicon spins of RFIC chips and minimize yield loss in large digital SoCs with RF and mixed signal parts while achieving the highest yield specially for RFICs in sub-90 nanometer nodes. The tutorial is intended for RFIC and SoC design engineers, Researchers and graduate students as well as product and marketing managers. The material will be given at an introductory level. So newcomers to the field will be welcome. The tutorial will cover the following main topics: Evolution of the wireless technology beyond 3G. The nanometer CMOS RF radio design problem. Built-in-self-test and self aware RFIC design. Digital calibration techniques. Case studies of an RF front-end for WiMAX/LTE.

5. Low Voltage Amplifiers Design Techniques

Edgar Sanchez Sinencio, TI J. Kilby Chair Professor, Director of the Analog and Mixed-Signal Center, Texas A&M University

Operational Amplifiers: Theory, Design and Practical Applications. This tutorial discusses the design techniques of amplifiers, beginning with fundamentals to low voltage amplifiers in modern small size technologies. The tutorial is intended for newcomers, designers that need to refresh fundamental techniques as well as for more experienced designers. A discussion on recent Op Amp design trends will be given. This tutorial is also addressed to graduate students as well as product and test managers. The tutorial will cover the following main topics: Classification of Amplifiers. Single-Input, Single Output. Differential Input, Single Output. Fully Differential. Low-Voltage (LV) Op Amp. LV Multiple Stage Amplifiers. Applications

6. Low-Power Design Techniques in Digital Systems

Prof. V. G. Oklobdzija, Professor Emeritus, University of California, Department of Electrical Engineering, University of Texas at Dallas

This talk addresses issues in designing digital systems operating with the minimal use of energy. A range of topics will be covered such as: power and energy fundamentals, power trends in relation to the device and voltage scaling, measures of power efficiency, the choice of the optimal design point, different circuit families for logic and for clocked storage elements and factors that influence power. Use of multiple power supply and threshold voltages and dynamic voltage scaling is also addressed. A set of comparison of different design points is presented.

7. Substrate Noise Mitigation in Systems on Chip

Shahab Ardalan, Gennum Corp., R&D-Analog Mixed Signal Group, University of Waterloo

As "System-on-Chip" designs are becoming popular, the substrate noise topic has attracted much attention since the past. Even today, significant research efforts are devoted to mitigate the impact of mostly digitally generated substrate noise on sensitive mixed-signal circuits. In mixed-signal circuits, complex and noisy digital circuits are integrated on the same substrate with noise-sensitive analog circuits. In fact, heavily integrated mixed-signal ICs are becoming ever so common. It is possible for the noise, generated by injected current into the common substrate, to result in functional failures of the analog and digital blocks. This tutorial makes a contribution in circuit and layout level substrate noise mitigation techniques. Different injection and reception mechanisms caused by a variety of effects may induce higher level of currents into the substrate. These effects have been modeled and verified experimentally by researchers. The complexity and accurate of a model depends on the intended application. However, most models are inadequate to accurately predict the substrate noise. Therefore, circuit and layout techniques are invariably employed to mitigate the generation as well as the impact of substrate noise.

MONDAY 3

<u>Registration Desk</u>	8:00 - 17:00 hrs.	
<u>Lunch</u>	13-20- 15:00 hrs	Kalmia Restaurant
<u>Opening Ceremony</u>	8:40-9:00	Condesa II Room
<u>Keynote Lecture</u>	9:00-10:30	Condesa II Room

Analog Design for Human-Centric Smart Living Technologies
Prof. Franco Maloberti, University of Pavia, Italy.

Technical Sessions

Oral Sessions

Time / Room	Condesa I-A	Condesa I-B	Condesa II	Ma. Beatriz	Ma. Mercedes	Ma. Fernanda
	Analog Cts.	Digital Cts	Student P.C.	Com & Wir	Bioeng Cts	Image Proc
10:30-10:50	107	78	33	298	85	75
10:50-11:10	249	148	35	390	325	109
11:10-11:30	23	228	90	77	346	141
11:30-11:50		293	137		403	234
	Analog Cts.	Digital Cts	Student P.C.	RF, MW Cts.	CAD & Lay	Linear & Non
12:00-12:20	157	197	152	56	146	25
12:20-12:40	277	276	253	110	203	63
12:40-13:00	29	424	265	166	324	180
13:00-13:20	440	20	285		269	
Lunch						
15:00-16:30	Poster	Poster		Poster	Poster	Poster
	DSP		Student P.C.	SoC & VLSI	Embedded S.	Amp & Comp
16:30-16:50		68	302	50	52	280
16:50-17:10		154	394	122	290	288
17:10-17:30		319	410	209	312	333
17:30-17:50		386	441	233		
17:50-18:10						

Poster Session

Pos.	Paper ID	Pos.	Paper ID	Pos.	Paper ID
1	41	17	362	33	131
2	183	18	45	34	214
3	26	19	61	35	404
4	47	20	190	36	69
5	49	21	198	37	458
6	79	22	356	38	459
7	82	23	418	39	
8	89	24	80	40	
9	96	25	93	41	
10	391	26	126	42	
11	309	27	128	43	
12	368	28	145	44	
13	382	29	150	45	
14	399	30	155	46	
15	242	31	16		
16	326	32	129		

Condesa I-A Room

Analog Circuits and Signal Processing 10:30 – 11:50

107 *A Spice Model for Magneto-Impedance Sensors*, Carlos A. De La Cruz Blas, Cristina Gómez-Polo, Alfonso Carlosena, Jesús Olivera, Public University of Navarra, Spain.

249 *Current Regenerative Schmitt Triggers with Tunable Hysteresis*, Fei Yuan, Ryerson University, Canada.

23 *Oscillation Controlled Electronic Systems Design Using Posicast-Based Pulse Pre-Shaping*, M. Rasoulzadeh, M. B. Ghaznavi-Ghouschi, Shahed University of Tehran, Iran.

Analog Circuits and Signal Processing 12:00 – 13:20

157 *High-Speed Transmitter for Fully Differential Current-Mode Polyquaternary Signaling Scheme*, Vijaya Sankara Rao P, Mrigank Sharad, Pradip Mandal, Indian Institute of Technology, India.

277 *Injection-Locked CMOS Active Transformer Voltage-Controlled Oscillators*, F. Yuan, Ryerson University, Canada.

29 *A 12nV/Hz Noise-Shaped Channel Select Filter for DVB-H Mobile-TV Tuners*, Ahmet Tekin, Hassan Elwan, Soliman Mamoud, Kenneth Pedrotti, Newport Media Incorporation, USA, German University of Cairo, Egypt, University of California Santa Cruz, USA.

440 *Psychoacoustic Bass Enhancement System on Reconfigurable Analog Signal Processor*, Leung Kin Chiu, David V. Anderson, Georgia Institute of Technology, USA

Condesa I-B Room

Digital Circuits 10:30 – 11:50

78 *A Quaternary Current Mode Bus Driver and Receiver Circuits*, Cheung Cheuk Kit, Cheong-Fat Chan, Chiu-Sing Choy, Kong-Pang Pun, The Chinese University of Hong Kong, Hong Kong.

148 *Manufacturable Low-Power Latches for Standard Tied-Double-Gate FinFET Technologies*, Sherif A. Tawfik, Volkan Kursun, University of Wisconsin-Madison, USA, The Hong Kong University of Science and Technology, Hong Kong.

228 *Speedup of a Large Word-Width High-Speed Asynchronous Multiply and Accumulate Unit*, Liang Zhou, Scott C. Smith, University of Arkansas, USA

293 *Hardware Implementations of the SHA-3 Candidates Shabal and CubeHash*, Markus Bernet, Luca Henzen, Hubert Kaeslin, Norbert Felber, Wolfgang Fichtner, Integrated Systems Laboratory ETH, Switzerland.

Digital Circuits 12:00 – 13:20

197 *A Novel All-Digital Phase-Locked Loop With Ultra Fast Frequency and Phase Acquisition*, Jun Zhao, Yong-Bin Kim, Northeastern University, USA

276 *A New Bit-Serial Architecture of Rank-Order Filter*, Takuya Yamamoto, Vasily G. Moshnyaga, Fukuoka University, Japan

424 *Performance of CNFET SRAM Cells under Diameter Variation Corners*, Zhe Zhang, Yanmin Liu, Jabulani Nyathi, José G. Delgado-Frias, Washington State University, USA.

20 *FinFET Technology Development Guidelines for Higher Performance, Lower Power, and Stronger Resilience to Parameter Variations*, Sherif A. Tawfik, Volkan Kursun, University of Wisconsin-Madison, USA, The Hong Kong Univ. of Science and Technology, Hong Kong.

Digital Signal Processing 16:30 – 17:50

68 *A Computation Structure for 2-D DCT Watermarking*, Shaofeng An, Chunyan Wang, Concordia University, Canada.

154 *Highly Directional and Selective Three Dimensional Adaptive IIR Filter*, Santosh Singh, Mehmet Celenk, Siemens Information Systems Ltd, India, Ohio University, USA.

319 *Complex Coefficient Adaptive IIR Notch Filter Tracking Characteristics*, Aloys Mvuma, Shotaro Nishimura, Takao Hinamoto, University of Dodoma, Tanzania, Shimane University, Japan, Hiroshima University, Japan.

386 *Low-Power Memory Addressing Scheme for Fast Fourier Transform Processors*, Xin Xiao, Erdal Oruklu, Jafar Saniie, Illinois Institute of Technology, USA.

Condesa II Room

Student Paper Contest 10:30 – 11:50

33 *Systematic Derivation of Reference Circuits for Wave Digital Modeling of Passive Linear Partial Differential Equations*, Christiane Leuer, Karlheinz Ochs, Ruhr-University Bochum, Germany

35 *Noise-Coupled Continuous-Time $\Delta\Sigma$ ADCs*, Yan Wang, Gabor C. Temes, Oregon State University, USA

90 *A Model of Multi-Walled Carbon Nanotube Interconnects*, Yau Xu, , USA, Ashok Srivastava, Ashwani K. Sharma, Louisiana State University, Electronics Foundations Group, AFRL/VSSE, USA

137 *Indirect Compensation Techniques for Three-Stage CMOS Op-amps*, Vishal Saxena, R. Jacob Baker, Boise State University, USA

Student Paper Contest 12:00 – 13:20

152 *Impulse Signal Generation and Measurement Technique for Cost-Effective Built-In Self Test in Analog Mixed-Signal Systems*, Wimol San-Um, Tachibana Masayoshi, Kochi University of Technology, Japan

253 *Hardware Implementation of Matrix Inversion for Raptor Decoder on Embedded System*, Todor Mladenov, Saeid Nooshabadi, Kiseon Kim, Gwangju Institute of Science and Technology, South Korea

265 *An Ultra Wideband Data Modulation Technique*, Gregorio Valdovinos F., Guillermo Espinosa F-V., Mario E. Magaña, National Institute of Astrophysics, Optics and Electronics, Mexico, Oregon State University, USA

285 $\Sigma\Delta$ *Time Interleaved Current Steering DAC with Dynamic Elements Matching*, Stefano Noli, Aldo Peña Perez, Edoardo Bonizzoni, Franco Maloberti, University of Pavia, Italy.

Student Paper Contest 16:30 – 17:50

302 *Analysis of the Electrical Performance of Multi-Coupled High-Speed Interconnects for SoP*, Victor H. Vega-González, Reydezel Torres-Torres, Adan S. Sánchez, INAOE, México, Intel Mexico Research Center, México.

394 *A DLL-Regulated SIMO Power Converter for DVS-Enabled Power-Aware VLSI Systems*, Rajdeep Bondade, Dongsheng Ma, The University of Arizona, USA

410 *A 5Gb/s 7-Channel Current-mode Imaging Receiver Front-end for Free-Space Optical MIMO*, Juan Zeng, Valencia Joyner, Jun Liao, Shengling Deng, Zhaoran Huang, Tufts University, USA, Rensselaer Polytechnic Institute, USA

441 *A Power-Efficient, High Data Rate Chaos-based Transceiver Design*, D. Majumdar, H. Leung, B. J. Maundy, University of Calgary, Canada

Ma. Beatriz Room

Communications and Wireless Systems 10:30-11:50

298 *RF Receiver and Transmitter for Insect Mounted Sensor Platform*, Joseph Duperre, Gordon Burgett, Rajesh Garg, Sunil P KhatriWest Virginia University, USA, Texas A&M University, USA

390 *Memory-Configuration and Memory-Bandwidth in the Sliding-Window (SW) Switch Architecture*, Alvaro Munoz, Cyrus D. Cantrell, University of Texas at Dallas, USA

77 *Design of a Costas Loop Down Converter*, Mike Roddewig, Seyed A. Zekavat, Saeid Nooshabadi, Michigan Technological University, USA, Gwangju Institute of Science and Technology, Republic of Korea

RF, Microwave Circuits 12:00-13:20

56 *Analysis of a 3-5 GHz UWB CMOS Low-Noise Amplifier for Wireless Applications*, Babak Ansari, Hosein Shamsi, Ali Shahhoseini, Islamic Azad University, Iran, K. N. Toosi University of Technology, Iran

110 *A 3-GHz Fully-Integrated CMOS Class-AB Power Amplifier*, Yuen Sum Ng, Lincoln Lai Kan Leung, Ka Nang Leung, The Chinese University of Hong Kong, Hong Kong

166 *Design Optimization of Voltage Controlled Oscillators in Consideration of Parasitic Capacitance*, Rui Murakami, Shoichi Hara, Kenichi Okada, Akira Matsuzawa, Tokyo Institute of Technology, Japan

SoC and VLSI 16:30-17:50

- 50 *Level shifting techniques for Mixed-Signal SoCs in low-voltage nanometer CMOS technologies*, Ayman Fayed, Iowa State University, USA
- 122 *Implementing Tree-Based Multicast Routing for Write Invalidation Messages in Networks-on-Chip*, Young Hoon Kang, Jeff Sondeen, Jeff Draper, University of Southern California, USA
- 209 *Electronic Design and Modeling of an Integrated Plasma Impedance Probe*, Magathi Jayaram, Mohamad El Hamoui, Chris Winstead, Edmund Spencer, Utah State University, USA
- 233 *A Low-Jitter Digital-to-Frequency Converter Based Frequency Multiplier with Large N*, Wickham Chen, Ping Gui, Liming Xiu, Southern Methodist University, USA, Texas Instruments, Inc., USA

Ma. Mercedes Room

Bioengineering Circuits and Systems 10:30-11:50

- 85 *A low power CMOS Biopotentiostat in a Low-Voltage 0.13 μm Digital Technology*, J. Colomer, P.Miribel-Català, A. Saiz-Vela, Ivón Rodríguez, J. Samitier, Universitat de Barcelona, Spain, Institut de Biotecnologia de Barcelona, Spain
- 325 *CMOS 12 bits 50kS/s Micropower SAR and Dual-Slope Hybrid ADC*, Xiang Fang, Vijay Srinivasan, Jack Wills, John Granacki, Jeff LaCoss, John Choma, University of Southern California, USA
- 346 *Automatic Heart Sound Analysis with Short-Time Fourier Transform and Support Vector Machines*, Wen-Chung Kao, Chih-Chao Wei, Jen-Jui Liu, Pei-Yung Hsiao, National Taiwan Normal University, Taiwan, National University of Kaohsiung, Taiwan
- 403 *Portable Transcorneal Electrical Stimulator System, Applied on Electrotherapy for Low Vision Patients*, D. Robles-Camarillo, L. Niño-de-Rivera, H. Quiroz-Mercado, M. J. López-Miranda, National Polytechnic Institute, Mexico, Denver Health Medical Center, University of Colorado, USA, Hospital Dr. Luis Sánchez Bulnes, APEC, México

CAD and Layout 12:00-13:20

- 146 *Logical Clustering for Fast Clock Skew Scheduling*, Liang Yang, Jiye Zhao, Baoxia Fan, Ge Zhang, Institute of Computing Technology and Chinese Academic of Sciences, China, Institute of Computing Technology, China
- 203 *Sensitivity Approach to Statistical Signal Integrity Analysis of Coupled Interconnect Trees*, Zhigang Hao, Guoyong Shi, Shanghai Jiao Tong University, China
- 324 *Design of Reusable CMOS OTAs using CAD Tools*, José Luis Chávez-Hurtado, Esteban Martínez-Guerrero, José Ernesto Rayas-Sánchez, Instituto Tecnológico y de Estudios Superiores de Occidente, México
- 269 *Decomposition-Based Multi-Objective Optimization of Second- Generation Current Conveyors*, I. Guerra-Gómez, E. Tlelo-Cuautle, T. McConaghy, G. Gielen, INAOE, México, Solido Design Automation Inc., Canada, Katholieke Universiteit Leuven, Belgium

Embedded Systems and Electronics 16:30-17:50

- 52 *A Novel Design Technique for Soft Error Hardening of Nanoscale CMOS Memory*, Sheng Lin, Yong-Bin Kim, Fabrizio Lombardi, Northeastern University, USA
- 290 *Analogue-Digital Interface for Low-Cost Sensors in Low-Power Sensing Networks*, Nicolas Medrano, A. Bayo, Belen Calvo, Santiago Celma, Maria Teresa Sanz, University of Zaragoza, Spain, Instituto Nacional Astrofísica, Óptica y Electrónica, México
- 312 *A Low-Power Multiplication Algorithm for Signal Processing Wireless Sensor Networks*, Ahmed Abdelgawad, Sherine Abdelhak, Soumik Ghosh, Magdy Bayoumi, University of Louisiana at Lafayette, USA

Ma. Fernanda Room

Image Processing and Multimedia Systems 10:30-11:50

- 75 *Algorithm of super-resolution in images and video sequences applying wavelets based on atomic functions*, F.Gomeztagle, V.F. Kravchenko, E. Escamilla, V. Ponomaryov, National Polytechnic Institute, Mexico, Institute of Radio Engineering and Electronics, Russia

109 *Edge-Adaptive Error Diffusion Using Chaotic Threshold Modulation*, Chung-Yen Su, You-Lin Sie, National Taiwan Normal University, Taiwan

141 *Analysis of QIM-Based Audio Watermarking using LDPC Codes*, Raúl Martínez-Noriega, Mariko Nakano, Brian Kurkoski, Kazuhiko Yamaguchi, Kingo Kobayashi, University of Electro-Communications, Japan, National Polytechnic Institute, Mexico, National Institute of Information and Communications Technology, Japan

234 *A Method for Edge Detection in Gray Level Images, based on Cellular Neural Networks*, José Antonio Medina Hernández, Felipe Gómez Castañeda, José Antonio Moreno Cadenas, CINVESTAV-IPN, México, Aguascalientes Autonomous University, México

Linear and Nonlinear Circuits and Systems, Theory and Applications 12:00-13:20

25 *Sinusoidal Oscillators and Multivibrators Are Not Separate Classes of Circuits*, I.M. Filanovsky, C.J.M. Verhoeven, University of Alberta, Canada, Electronics Research Laboratory, TU Delft, The Netherlands

63 *The Transient Response of a Duffing Resonator following a Parameter Change*, Chenchen Deng, Steve Collins, University of Oxford, United Kingdom

180 *Hybrid Equivalent Circuit, an Alternative to Thevenin and Norton Equivalents, Its Properties and Applications*, Reza Hashemian, Northern Illinois University, USA

Amplifiers and Comparators 16:30-17:50

280 *Design Procedure and Performance Potential for Operational Amplifier using Indirect Compensation*, Vaibhav Kumar, Degang Chen, Texas Instrument, USA, Iowa State University, USA

288 *Low-Voltage CMOS Cross-Quad Implementation based on Dynamic Positive Feedback*, Belen Calvo, Jaime Ramirez-Angulo, Antonio Lopez-Martin, Ramon G. Carvajal, University of Zaragoza, Spain, New Mexico State University, USA, Univ. Pública de Navarra, Spain, University of Seville, Spain

333 *A Precision Architecture For High-Speed Amplifier Applications*, Donald T. Comer, Brigham Young University, USA

Condesa III Room

Poster Session 15:00-16:30

41 *Initialization of linear multistep methods in multidimensional wave digital models*, Georg Hetmanczyk, Karlheinz Ochs, Ruhr-University, Germany

183 *A CMOS Negative Supply for Large Dynamic Range High-Bandwidth Analog Circuits*, Xiong Liu, Alan N. Willson, Jr., University of California, USA

26 *A CMOS Voltage Reference Using Compensation Of Mobility and Threshold Voltage/Temperature Effects*, I.M. Filanovsky, Brenda Bai, Brian Moore University of Alberta, Canada, Scanimetrics Inc., Canada

47 *Modeling of CFOA Based Non-Inverting Amplifier Using Standard Hardware Description Language*, Rasha E. El-Queseny, Soliman A. Mahmoud, Magdy M. Ibrahim, The German University in Cairo, Egypt, Ain Shams University, Egypt

49 *Balanced Transconductor-C Ladder Filters With Improved Linearity*, Antonio Carlos M. de Queiroz, Federal University of Rio de Janeiro, Brazil

79 *Fully Balanced Voltage Differencing Buffered Amplifier and its Applications*, Viera Biolkova, Zdenek Kolka, Dalibor Birolek Brno Univ. of Technology, Czech Republic, FVT, Univ. of Defence. Czech Republic

82 *Comparative Study on the Effects of PVT Variations Between a Novel All-MOS Current Reference and Alternative CMOS Solutions*, Jindrich Windels, Christophe Van Praet, Herbert De Pauw, Jan Doutreloigne, Ghent University, Belgium

89 *A Flexible Hardware Encoder for Systematic Low-Density Parity-Check Codes*, Hemesh Yasotharan, Anthony Chan Carusone, University of Toronto, Canada

96 *A Type III Fast Locking Time PLL with Transconductor-C Structure*, Habib Adrang, Hossein Miar Naeimi, Babol University of Technology, Iran

391 *A Modified Branin Model of Lossless Transmission Lines*, Josef Dobeš, Libor Sláma, Czech Technical University in Prague, Czech Republic

- 309 *Design and Implementation of the Baseband Section for a 900MHz Passive Tag in a 0.5 μ m CMOS Process*, Omar R. Ávila-López, R. Parra-Michel, F. Sandoval-Ibarra, M. Aguirre-Hernández, CINVESTAV Guadalajara, México, Universidad Panamericana, México, Intel Corporation, Mexico
- 368 *Coding Efficiency for Different Switched-Mode RF Transmitter Architectures*, Thomas Blocher, Peter Singerl, Graz University of Technology, Austria, Infineon Technologies Austria AG, Austria
- 382 *Communication infrastructures to facilitate regional voltage control of active radial distribution networks*, Qiang Yang, Javier A. Barria, Carlos A. Hernandez Aramburo, Imperial College London, United Kingdom
- 399 *A Tunable Pulse Generator for Sub-GHz UWB Systems*, Youngjoong Joo, Hyunseok Kim, Sungyong Jung University of Texas at San Antonio, USA, ETRI, Republic of Korea, University of Texas at Arlington, USA
- 242 *Design And Implementation of an Android*, Norma Elva Chávez Rodríguez, Rodrigo Savage, José Iván Guevara Juarez, Marcial Roberto Leyva Fernández, Universidad Nacional Autónoma de México, México
- 326 *Trajectory Tracking Control for the Planar Dynamics of a Thrust Vektored Airship*, G. Murguía-Rendon, H. Rodríguez-Cortés, M. Velasco-Villa, CINVESTAV-IPN, México
- 362 *Stand-alone station for deep space objects astrophotography*, R. Suszynski, Koszalin University of Technology, Poland
- 45 *Complex Bandpass $\Delta\Sigma$ AD Modulator with Noise-coupled Image Rejection*, Hao San, Haruo Kobayashi, Gunma University, Japan
- 61 *A Continuously Trimmable Comparator-based Gain Stage*, R. Rieger, L.-S. Chang, National Sun Yat-Sen University, Taiwan
- 190 *Improved Delta Sigma Modulators for High Speed Applications*, David Gautier, Michel Robbe, Stephan Doucet, Renaud Lemoine, Smail Bachir, Claude Duvanaud, ACCO SEMICONDUCTOR, France, Université de Poitiers, France
- 198 *A Multi-bit Sigma-Delta Modulator Using Ratio-Independent Feedback DAC*, Yu Song, Eric C. Moule, University of Rochester, USA, ADVIS, Inc., USA
- 356 *Low Power Current Mode Pipelined A/D Converter*, Krzysztof Wawryn, Robert Suszyński, Bogdan Strzeszewski, Koszalin University of Technology, Poland
- 418 *A 5-Bit 10GS/s 65nm Flash ADC with Feedthrough Cancellation Track-and-Hold Circuit*, Gang Chen, Yifei Luo, Allen Drake, Kuan Zhou, University of New Hampshire, USA
- 80 *Pulse Width Variation Tolerant Clock Tree Using Unbalanced Cells for Low Power Design*, Tarun Chawla, Sebastien Marchal, Amara Amara, Andrei Vladimirescu, STMicroelectronics, France, Institute Superior d'Electronique de Paris, France
- 93 *Low-Power FPGA Routing Switches Using Adaptive Body Biasing Techniques*, Kundan Nepal, George V. Leming, Bucknell University, USA, Bucknell University, USA
- 126 *A Circuit Design and Fabrication Approach to Address Global Process Variation*, Ardavan Aryanpour, Glenn E. R. Cowan Concordia University, Canada
- 128 *A Survey on Leakage Control Techniques in Wide-OR Domino Circuits*, Farhad Haj Ali Asgari, Majid Ahmadi, Jonathan Wu, University of Windsor, Canada
- 145 *Optimization of Oversampling Data Recovery*, Zdenek Kolka, Michal Kubicek, Dalibor Bielek, Viera Biolkova, Brno University of Technology, Czech Republic
- 150 *An Image Combiner and Acquisition Interface for Space Remote Sensing Applications*, Tsan-Jieh Chen, Herming Chiueh, Hann-Huei Tsai, Chin-Fong Chiu, National Chiao-Tung University, Taiwan, National Applied Research Laboratories, Taiwan
- 155 *Design of Low Power Precharge-Evaluation Based One Bit Adder Cell*, Krashna Nand Mishra, ATLab Inc., Republic of Korea
- 16 *3D Imaging Algorithm and Implement for Through-Wall Synthetic Aperture Radar*, Jiabing Zhu, Liang Tao, Yi Hong, East China Research Institute of Electronic Engineering, China, Anhui University, China
- 129 *Fast Mutual Coupling Compensation Algorithm for Large Adaptive Antenna Array*, Viktor V. Zaharov, Angel Lambert Lobaina, Jaime L. Rodriguez, Ramon Albandoz Soto, Polytechnic University of Puerto Rico, Puerto Rico, Universidad Anáhuac Norte, México
- 131 *Conjugate Gradient Based Complex Block LMS Employing Time-Varying Optimally Derived Stepsizes*, Ying Liu, Raghuram Ranganathan, Matthew T. Hunter, Wasfy B. Mikhael, University of Central Florida, USA, DME Corporation, USA

214 *Digital Beam-forming Implementation for Downlink Smart Antenna System*, Reza Abdolee, Wei-Ping Zhu, Mohamad Sawan, Concordia University, Canada, Ecole Polytechnique de Montréal, Canada

404 *Adaptive Noise Canceller using LMS algorithm with codified error in a DSP*, J. Gerardo Avalos, Daniel Espinobarro, Jose Velazquez, Juan C. Sanchez, National Polytechnic Institute, Mexico

69 *Multiple-filtering process and its application in edge detection*, Jing Li, Chunyan Wang, Concordia University, Canada

458 *An Electric Energy Distribution Systems Protection Microprocessor Based Relay*, Israel Olguin Carbajal, Enrique Cisneros Sedano, Blanca Alicia Rico Jiménez Sistemas Eléctricos de Potencia Computarizada S.A. de C.V., México, Instituto Politécnico Nacional, México

459 *Series Wound DC Motor Modeling and Simulation, Considering Magnetic, Mechanical and Electric Power Losses*, J. S. Valdez Martínez, P. Guevara López, J. J. Medel Juárez, Instituto Politécnico Nacional, México

TUESDAY 4

<u>Registration Desk</u>	08:00 17:00 hrs.	
<u>Lunch</u>	13-20- 15:00 hrs	Kalmia Restaurant
<u>Congress Banquet</u>	19:00 hrs	Peninsula Ballroom
<u>Keynote Lecture</u>	9:00-10:30 hrs	Condesa II Room

Vector Order Statistics and Fuzzy Set Approaches in 3D Digital Processing of Multichannel Images and Video Sequences Employing DSP/FPGA
Dr. Volodymyr Ponomaryov, National Polytechnic Institute of Mexico, ESIME-Culhuacan

Technical Sessions

Oral Sessions

Time / Room	Condesa I-A	Condesa I-B	Condesa II	Ma. Beatriz	Ma. Mercedes	Ma. Fernanda
	Analog Cts	Digital Cts		Com & Wir	Bioeng Cts	Image Proc
10:30-10:50	185	102		72	87	101
10:50-11:10	289	238		266	339	279
11:10-11:30	380	212		337	371	308
11:30-11:50	420	213		429	431	437
	Data Conv	DSP	RF, MW	Reconfig C.	CAD & Lay	Linear & Non
12:00-12:20	55	58	245	407	130	201
12:20-12:40	187	83	74	450	299	477
12:40-13:00	331	240	342		246	127
13:00-13:20		330			387	
	Lunch	Lunch	Lunch	Lunch	Lunch	Lunch
15:00-16:30	Poster	Poster		Poster	Poster	Poster
	Data Conv	DSP	Real Time S.	Control Syst	SoC VLSI	
16:30-16:50	38	009	478	59	243	
16:50-17:10	142	247	457	384	256	
17:10-17:30	281	438	466	300	271	
17:30-17:50	341	454	467	304	272	

Poster Session (Condesa III Room)

Pos.	Paper ID	Pos.	Paper ID	Pos.	Paper ID
1	275	17	115	33	204
2	320	18	135	34	268
3	92	19	327	35	465
4	140	20	98	36	
5	174	21	111	37	
6	175	22	164	38	
7	307	23	181	39	
8	28	24	196	40	
9	149	25	8	41	
10	158	26	211	42	
11	215	27	217	43	
12	223	28	311	44	
13	39	29	347	45	
14	120	30	46	46	
15	159	31	200	47	
16	106	32	202		

Condesa I-A Room

Analog Circuits and Signal Processing 10:30 – 11:50

185 A 3 mW/GHz Near 1-V VCO with Low Supply Sensitivity in 0.18- μ m CMOS for SoC Applications, Xiong Liu, Alan N. Willson, Jr., University of California, USA

289 A Low-Power High-Sensitivity CMOS Voltage-to-Frequency Converter, Belen Calvo, Nicolas Medrano, Santiago Celma, Maria Teresa Sanz, University of Zaragoza, Spain, Instituto Nacional Astrofísica, Óptica y Electrónica, México

380 Micropower Class AB CMOS Current Conveyor Based on Quasi-Floating Gate Techniques, Antonio J. Lopez-Martin, Lucía Acosta, Jose M. Algueta, Jaime Ramirez-Angulo, Ramon G. Carvajal, Public University of Navarra, Spain, Universidad de Sevilla, Spain, New Mexico State University, USA

420 Threshold-Based Voltage Reference with pn- Junction Temperature Compensation, Yen-Ting Wang, Randall L. Geiger, Shu-Chuan Huang, Tatung University, Taiwan, Iowa State University, USA

Data Converters 12:00 – 13:20

55 Novel sampling-timing background calibration for time-interleaved A/D converters, Takashi Oshima, Tomomi Takahashi, Taizo Yamawaki, Hitachi Ltd., Central Research Laboratory, Japan

187 A Pipelined ADC Architecture for Low-Voltage CMOS Applications, Kent D. Layton, Donald T. Comer, ON Semiconductor, USA, Brigham Young University, USA

331 A K-Delta-1-Sigma Modulator for Wideband Analog to Digital Conversion, Vishal Saxena, Kaijun Li, Geng Zheng, R. Jacob Baker, Boise State University, USA

Data Converters 16:30 – 17:50

38 Wideband Σ ADCs Using Direct-Charge-Transfer Adder, Yan Wang, Gabor C. Temes, Oregon State University, USA

142 An On-chip Ramp Generator for Single-Slope Look Ahead Ramp (SSLAR) ADC, Sakkarapani Balagopal, Suat U. Ay, University of Idaho, USA

281 A Σ CMOS ADC with 80-dB Dynamic Range and 31-MHz Signal Bandwidth, Mohamed Aboudina, Behzad Razavi, University of California, USA

341 An Oversampling Digital Pixel Sensor with a Charge Transfer DAC Employing Parasitic Capacitances, Danijel Maricic, Zeljko Ignjatovic, Mark F. Bocko, University of Rochester, USA

Condesa I-B Room

Digital Circuits 10:30 – 11:50

102 An Efficient Implementation of 1-D Median Filter, Vasily G. Moshnyaga, Koji Hashimoto, Fukuoka University, Japan

238 Delay-Compensation Techniques for Ultra-Low-Power Subthreshold CMOS Digital LSIs, Yuji OSAKI, Tetsuya Hirose, Kei matsumoto, Nobutaka Kuroki, Masahiro Numa, Kobe University, Japan

212 Simplified 3.3v Tolerance Circuit for 2.5v I/O Design in Pci-X Signaling Environment, Akshaykumar Salimath, Satyam Mandavilli, International Institute of Information Technology, India

213 A Digital-to-Frequency Converter Using Redundant Signed Binary Addition, Wickham Chen, Mitchell A. Thornton, Ping Gui, Southern Methodist University, USA

Digital Signal Processing 12:00 – 13:20

58 Design of Least-Square GCF Compensation Filter, Alfonso Fernandez-Vazquez, Gordana Jovanovic Dolecek, National Institute of Astrophysics, Optics, and Electronics, Mexico, San Diego State University, USA

83 A Novel Farrow Structure with Reduced Complexity, Matthew T. Hunter, Wasfy B. Mikhael, DME Corporation. USA, University of Central Florida, USA

240 *Realization of a Recursive 3-D Cone Filter for Video Processing Applications*, Sam Schauland, Jörg Velten, Anton Kummert, University of Wuppertal, Germany

330 *A Wavelet-Based 128-bit Key Generator Using Electrocardiogram Signals*, H. A. Garcia-Baleon, V. Alarcon-Aquino, O. Starostenko, Universidad de las Américas Puebla, México

Digital Signal Processing 16:30 – 17:50

9 *All-Zero Block Detection in VC-1*, Hisham Sliman, Mohamed El-Sharkawy, Paul Salama, Maher Rizkalla, Salwa El-Ramly, Purdue School of Engineering and Technology, USA, German University, Egypt, Ain Shams University, Egypt

247 *Comparison of Techniques for L2-Sensitivity Minimization Under L2-Scaling Constraints in State-Space Digital Filters*, Takao Hinamoto, Kensuke Kai, Wu-Sheng Lu Hiroshima University, Japan, University of Victoria, Canada

438 *An Adaptive Fast and Efficient Spatial Error Concealment Technique for Block-Based Video Coding Systems*, Nourhan El Beheiry, Mohamed El Sharkawy, Mona Lotfy, Said Elnoubi, Alexandria University, Egypt, German University in Cairo, Egypt, Purdue School of Engineering and Technology, USA

454 *Design of Multiplierless Decimation Filters Based on Cyclotomic Polynomials*, Massimiliano Laddomada, Fabio Mesiti, Marina Mondin, Texas A&M University, USA, Politecnico di Torino, Italy

Condesa II Room

RF, Microwave Circuits 12:00 – 13:20

245 *A Differential Common-Gate Class-E Power Amplifier with Positive-Negative Feedback*, Sherif A. Mohamed, Yiannos Manoli, Maurits Ortmanns, University of Freiburg, Germany, University of Ulm, Germany

74 *A 0-90° Low-Loss Miniaturized Reflective-Type CMOS Phase Shifter Using Active Inductors*, Kamran Entesari, Ahmad Reza Tavakoli, Texas A&M University, USA

342 *A 1-V 14.6-dB gain LNA for WiMAX 2~6 GHz Applications*, Chia-Wei Chang, Zhi-Ming Lin, National Changhua University of Education, Taiwan

Real Time Systems Modeling and Applications 16:30 – 17:50

478 *An Alaryngeal Speech Enhancement Method Based on ADPCM Approach*, Agustin Razo-Chavez, Mariko Nakano-Miyatake, Hector Perez-Meana, National Polytechnic Institute, México

457 *A Metric for the Evaluation of the Efficiency in Scheduler of Concurrent Real-Time Tasks*, Pedro Guevara López, José Carlos Quezada Quezada, Asdrúbal López Chau, Instituto Politécnico Nacional, México, Universidad Autónoma del Estado de Hidalgo, México, Instituto Politécnico Nacional - CICATA, México

466 *Modeling and Reconstruction of the statistical data from a System Electronic Application for Administrative Management in IPN through the filter of Kalman*, P. Guevara López, J.J. Medel, M. T. Zagaceta, A. T. Ramirez Romero, National Polytechnic Institute, Mexico

467 *Description of Adaptive Fuzzy Filtering Using The DSP TMS320C6713*, Vázquez Burgos L. S, Garcia Infante J. C., Sánchez Garcia J. C., National Polytechnic Institute, Mexico

Ma. Beatriz Room

Communications and Wireless Systems 10:30-11:50

72 *Perturbation Analysis of Whitening-Rotation-based Semi-Blind MIMO Channel Estimation*, Feng Wan, Wei-Ping Zhu, M.N.S. Swamy, Concordia University, Canada

266 *Optimal Resource Allocation for Wireless Video Sensors with Power-Rate-Distortion Model of Imager*, Malisa Marijan, Wendi Heinzelman, Gaurav Sharma, Zeljko Ignjatovic, University of Rochester, USA

337 *Sensitivity Analysis of Direct Conversion Receivers to Analog-to-Digital Converter Performance*, Kye-Shin Lee, Hochul Kim, Joonsung Park, Sun Moon University, Korea, Texas Instruments Inc., USA, University of Texas at Austin, USA

429 *A Hybrid Algorithm and its Re-configurable Architecture for MIMO Detector*, Luo Dan, Chi-Ying Tsui, The Hong Kong University of Science & Technology, Hong Kong

Reconfigurable Computing 12:00-13:20

407 *Testing Faults in SRAM Memory of Virtex-4 FPGA*, Mohammed Niamat, Manoj Lalla, Junghwan Kim, University of Toledo, USA

450 *A multi-context programmable optically reconfigurable gate array without a beam splitter*, Shinya Kubota, Minoru Watanabe, Shizuoka University, Japan

Control Systems, Mechatronics and Robotics 16:30-17:50

59 *Data Processing from a Laser Range Finder Sensor for the Construction of Geometric Maps of an Indoor Environment*, Marcos Ogaz, Mario Chacón, Rafael Sandoval, Chihuahua Institute of Technology, México

384 *Stabilization of High-Order Systems with Delay Using a Predictor Schema*, Y. Pedraza-Beltran, O. Gonzalez-Nagera, B. del Muro-Cuéllar, Instituto Politécnico Nacional, México

300 *Experimental Comparison of Non-collision Strategies in Multi-Agent Robots Formation Control*, E. G. Hernández-Martínez, E. Aranda-Bricaire, CINVESTAV, México

304 *Concept validation of a MEMS powered, automatic multichannel pipetting device*, Ana L. Quintanar-Meléndez, C. Annael Orozco-Díaz, Rogelio Bustamante-Bello, José R. Alvarez-Bada, M. Karla Muguierza-Jiménez, Jessica Nava-Rojas, Instituto Tecnológico y de Estudios Superiores de Monterrey, Ciudad de México

Ma. Mercedes Room

Bioengineering Circuits and Systems 10:30-11:50

87 *Dynamic Pupil Reacting to Incident Light Dedicated to Ocular Implants*, Mohamad Wehbe, Mona Safi-Harb, Mohamad Sawan, Ecole Polytechnique de Montreal, Canada

339 *An Adaptive System to Stimulate Culture Cells*, Ernesto Paredes Martínez, Luis Niño de Rivera O, Atlántida M. Raya-Rivera, Daniel Robles Camarillo, Raquel Vargas Jimenez, National Polytechnic Institute, Mexico, Federico Gomez Childhood Mexican Hospital, México

371 *A ± 9 V Fully Integrated CMOS Electrode Driver for High-Impedance Microstimulation*, Sébastien Ethier, Mohamad Sawan, El Mostapha Aboulhamid, Mourad El-Gamal, Ecole Polytechnique, Canada, Université de Montreal, Canada, McGill University, Canada

431 *On-Chip Intrinsic Evolution Methodology for Sequential Logic Circuit Design*, Fan Xiong, Nader I. Rafla, Boise State University, USA

CAD and Layout 12:00-13:20

130 *Design of a CMOS Second Order Band-Pass Continuous Time Filter using Numerical Optimization*, Luis Nathán Pérez-Acosta, José Ernesto Rayas-Sánchez, Intel - Guadalajara Design Center, México, Instituto Tecnológico y de Estudios Superiores de Occidente, México

299 *Post-CTS Clock Skew Scheduling with Limited Delay Buffering*, Jianchao Lu, Baris Taskin, Drexel University, USA

246 *Computing Optimum Sizes of a Voltage Follower using Fuzzy Sets*, S. Polanco-Martagón, G. Flores-Becerra, E. Tlelo-Cuautle, Instituto Tecnológico de Puebla, México, INAOE, Mexico

387 *Capacitive Load Balancing for Mobius Implementation of Standing Wave Oscillator*, Vinayak Honkote, Baris Taskin, Drexel University, USA

SoC and VLSI 16:30-17:50

243 *Hybrid Memory Architecture for Regular Expression Matching*, Cheng-Hung Lin, National Taiwan Normal University, Taiwan

256 *High-Frequency Interconnect Modeling for Global Signal Networks*, O. Gonzalez-Diaz, M. Linares-Aranda, R. Torres-Torres, Instituto Nacional de Astrofísica, Óptica y Electrónica, México

271 *The Implementation and Design Methodology of a Quad-Core Version Godson-3 Microprocessor*, Baoxia Fan, Liang Yang, Zhuo Gao, Feng Zhang, Ru Wang, Institute of Computing Technology, China, Graduate University of Chinese Academy of Sciences, China, Institute of Computing Technology, China

272 *On Chip LC Resonator Circuit Using an Active Inductor for Adiabatic Logic*, Yasuhiro Takahashi, Nazrul Anuar, Shun-ya Nagano, Toshikazu Sekine, Michio Yokoyama, Gifu University, Japan, Yamagata University, Japan

Ma. Fernanda Room

Image Processing and Multimedia Systems 10:30-11:50

101 *Modification to Fast and Efficient Spatial Error Concealment Technique for Block-Based Video Coding Systems*, Nourhan El Beheiry, Mohamed El Sharkawy, Mona Lotfy, Said Elnoub, Alexandria University, Egypt, Purdue School of Engineering and Technology, USA and, German University in Cairo, Egypt

279 *3D Color Video Conversion from 2D Video Sequence Using Stereo Matching Technique*, Eduardo Ramos-Diaz, Miguel Cruz-Irison, Luis Nino-de-Rivera, Volodymyr Ponomaryov, National Polytechnic Institute, Mexico

308 *A Theoretical Exposition to Apply LAMDA Methodology to Vector Quantization*, Enrique Guzmán, Juan G. Zambrano, Antonio Orantes, Oleksiy Pogrebnyak, Universidad Tecnológica de la Mixteca, México, National Polytechnic Institute, Mexico

437 *Low Power Implementation of DCT for On-Board Satellite Image Processing Systems*, S. Vijay, D. Anchit, Arizona State University, USA

Linear and Nonlinear Circuits and Systems, Theory and Applications 12:00-13:20

201 *An NMOS Low Dropout Voltage Regulator with Switched Floating Capacitor Gate Overdrive*, Daniel Camacho, Ping Gui, Paulo Moreira, Southern Methodist University, USA, CERN, Switzerland

477 *On the Mode Analysis of Coupled Oscillators*, Ahmad Mirzaei, Mohammad E. Heidari, Broadcom Corporation, USA, Wilinx Corporation, USA

127 *Two-Dimensional Laplace, Hankel, and Mellin Transforms of Linear Time-Varying Systems*, Shervin Erfani, Nima Bayan, University of Windsor, Canada, Esys Corporation, USA

Condesa III Room

Poster Session 15:00-16:30

275 *Analog Current-Mode Implementation of a Logistic-Map Based Chaos Generator*, Juan López-Hernández, Alejandro Díaz-Méndez, Rubén Vázquez-Medina, Ruben Alejos-Palomares, Instituto Politécnico Nacional, México, Instituto Nacional de Astrofísica Óptica y Electrónica, México & Instituto Politécnico Nacional, México, Universidad de las Americas, Puebla, México

320 *A Low Area Pipelined 2-D DCT Architecture for JPEG Encoder*, Qihui Zhang, Nan Meng, Henan University, China, Beijing University of Posts and Telecommunications, China

92 *Fuzzy Technique for Image Enhancement Using B-spline*, A. Anzueto-Rios, J. A. Moreno-Cadenas, F. Gómez-Castañeda, CINVESTAV-IPN, México

140 *Multistable Cellular Neural Networks and Their Application to Image Decomposition*, José Antonio Medina Hernández, Felipe Gómez Castañeda, José Antonio Moreno Cadenas, CINVESTAV-IPN, Aguascalientes Autonomous University, México

174 *An Interconnection Architecture for Integrated and Fire Neuromorphic Multi-Chip Networks*, Fausto Sargeni, Vincenzo Bonaiuto, University of Rome "Tor Vergata", Italy

175 *Programmable Non-Linearity for Neural Networks Applications*, Fausto Sargeni, Vincenzo Bonaiuto, University of Rome "Tor Vergata", Italy

307 *Neural Fuzzy Digital Filtering: Properties*, J. C. García Infante, J. C. Sánchez García, J. J. Medel Juárez, National Polytechnic Institute, Mexico

28 *Femtosecond Laser Blackening of Metals*, Anatoliy Y. Vorobyev, Chunlei Guo, University of Rochester, USA

149 *A Supply and Process-Insensitive 12-Bit DPWM for Digital DC-DC Converters*, Huey Chian Foong, Meng Tong Tan, Yuanjin Zheng, Nanyang Technological University, Singapore, Institute of Microelectronics, Singapore

158 *Low-Ripple Skipping-based Regulation System for a Two-Phase Voltage Doubler Charge Pump*, Albert Saiz-Vela, Pere Miribel-Català, Jordi Colomer, Josep Samitier, University of Barcelona, Spain

- 215 *A Class of Optimal Multilevel Inverters Based on Sectionalized PWM (S-PWM) Modulation Strategy*, Hirak Patangia, Dennis Gregory, University of Arkansas, USA
- 223 *Current-mode DC-DC Buck Converter with Reliable Hysteretic-Mode Control and Dual Modulator for Fast Dynamic Voltage Scaling*, Jungmoon Kim, Hyunho Chu, Chulwoo Kim, Korea University, Korea
- 39 *Design Optimization and Modeling of on-Chip RF Inductors in 0.13 μ m and 90nm Standard CMOS*, Fan Zhang, Zhihua Wang, Xin Wang, He Tang, Qiang Fang, Albert Wang, Gary Zhang, Xingang Wang, Wei Chen, Lee Yang, Bin Zhao, Tsinghua University, China, University of California, USA, Skyworks Solutions Inc., USA, Semiconductor Manufacturing International Corporation, China, Freescale Semiconductor, USA
- 120 *A CMOS Receiver with Single RF Channel for SMILE Applications*, C. E. Capovilla, A. Tavora, L. C. Kretly, University of Campinas, Brazil
- 159 *CMOS Colpitts LC Reference Oscillator with 70ppm Absolute Frequency Accuracy within 0 – 80 °C*, Erdogan Ozgur Ates, Devrim Yilmaz Aksim, Pinar Basak Basyurt, Mikroelektronik RD Design Center, Turkey, Istanbul Technical University, Turkey
- 106 *High-performance and Low-bandwidth Architecture of H.264 Motion Estimation Circuit for 1080HD Video*, Soojin Kim, Hoyoung Chang, Seonyoung Lee, Kyeongsoon Cho, Hankuk University of Foreign Studies, Republic of Korea
- 115 *Performance Analysis of Future System-on-Fpga Topology Candidates*, Nasser Alaraje, J. E. DeGroat, Michigan Technological University, USA, Ohio State University, USA
- 135 *Interconnect Technique for Sub-Threshold Circuits using Negative Capacitance Effect*, Md. Sajjad Rahaman, Masud H Chowdhury, University of Illinois at Chicago, USA
- 327 *Fingerprint Verification applying Invariant Moments*, J. Leon, G. Sanchez, G. Aguilar, L. Toscano, H. Perez, J. M. Ramirez, National Polytechnic Institute, Mexico, National Institute for Astrophysics, Optics, and Electronics, México
- 98 *A Nanowatt Cascadable Delay Element for Compact Power-on-Reset (POR) Circuits*, Suat U. Ay, University of Idaho, USA
- 111 *A CMOS Low Complexity Gaussian Pulse Generator for Ultra Wideband Communications*, Gregorio Valdovinos Fierro, Guillermo Espinosa Flores-Verdad, National Institute of Astrophysics, Optics and Electronics, Mexico
- 164 *The Design of Sub-threshold Reference Circuit Using Resistor Temperature Compensation*, Luo Li, Cai Xiaowei, Li Zheyang, Beijing Jiao Tong University, China, Beijing Union University, China
- 181 *A Modified Charging Algorithm for Comparator-Based Switched-Capacitor Circuits*, Kim-Fai Wong, Sai-Weng Sin, Seng-Pan U, R.P. Martins, University of Macau, China, Instituto Superior Técnico de Lisbon, Portugal
- 196 *Limitations of the Phase-to-Frequency-Detector in Fractional Frequency Synthesizers.*, Victor R. Gonzalez-Diaz, Guillermo Espinosa F. V., Miguel A. Garcia-Andrade, National Institute for Astrophysics Optics and Electronics, México, Universidad Autónoma de Baja California, Mexico
- 8 *A Pseudo Rail-to-Rail Chopper-Stabilized Instrumentation Amplifier in 0.13 μ m CMOS*, Fuding Ge, Intel Corporation, USA
- 211 *A Self Tuning System for On-Die Terminators in Current Mode Off-Chip Signaling*, Edgar López-Delgado, Alejandro Díaz-Méndez, Miguel A. Garcia-Andrade, Mario E. Magaña, Franco Maloberti, National Institute for Astrophysics, Optics and Electronics, México, Universidad Autónoma de Ciudad Juárez, Mexico, Oregon State University, USA, University of Pavia, Italy
- 217 *A Multiple Loop Feedback Gm-C Bandpass Filter for Wavelet Transform Implementation*, Wenshan Zhao, Yichuang Sun, Xi Zhu, Yigang He, University of Hertfordshire, United Kingdom, Hunan University, China
- 311 *Floating-Gate Energy Recovery Logic*, Luis F. Cisneros-Sinencio, Alejandro Diaz-Sanchez, Jaime Ramirez-Angulo, Carlos A. Gracios-Marin, National Institute for Astrophysics, Optics and Electronics, México, New Mexico State University, USA, Puebla Institute of Technology, Mexico
- 347 *Exploration of Switching Activity Behavior of Addition Algorithms*, Dursun Baran, Mustafa Aktan, Hossein Karimiyan, Vojin G. Oklobdzija, University of Texas at Dallas, USA
- 46 *A tunable band-pass filter using a complex-arithmetic heterodyne approach*, Michael A. Soderstrand, Grace Yoona Cho, DeVry University Oklahoma City Center, USA, Tellabs Wireless Group, USA
- 200 *A Robust Detection in the Presence of a Strong Unwanted Periodical Signal with Unknown Nonstationary Power*, V. Golikov, O. Lebedeva, F.J. Miguel Reyes, Universidad Autónoma del Carmen, México

202 *Power Aware Combination of Transposed-Form and Direct-Form FIR Polyphase Decimators for Sigma-Delta ADCs*, Ahmed Shahein, Markus Becker, Niklas Lotze, Yiannos Manoli, University of Freiburg, Germany

204 *Blind ISI Correction by Using CMA*, Jorge Omar Pérez, Hilda Noemí Ferrão, Claudia F. Sayago, Wenceslao Novotny, Universidad Nacional de Tucumán, Argentina

268 *CBIR for Image-Based Language Learning within Mobile Environment*, O. Starostenko, R. Contreras Gómez., V. Alarcon-Aquino, O. Sergiyenko, Universidad de las Américas, Puebla, México, Baja California Autonomous University, México

465 *Measuring the efficiency of Schedulers for Concurrent Real-time Tasks in Uniprocessor Systems*, Pedro Guevara López, Raúl J. Sandoval Gómez, Fernando Vázquez Torres, Instituto Politécnico Nacional, México

WEDNESDAY 5

Registration Desk

08:00 17:00 hrs.

Lunch

13-.20- 15:00 hrs

Kalmia Restaurant

Keynote Lecture

9:00-10:30 hrs

Condesa II Room

Reconfigurable Signal Processing in Software Defined Radio and Instrumentation

Matthew T. Hunter, Ph.D. Chief Research Scientist Signal Processing and Communications DME Corporation

Dr Wasfy Mikhael, Fellow IEEE, Professor School of Electrical Engineering and Computer Science, University of Central Florida

Technical Sessions

Oral Sessions

Time / Room	Condesa I-A	Condesa I-B	Condesa II	Ma. Beatriz	Ma. Mercedes	Ma. Fernanda
	Analog Cts	Digital Cts		MEMS/NANO	Neural/ Fuzzy	SoC VLSI
10:30-10:50	193	143		355	263	434
10:50-11:10	306	165		453	301	91
11:10-11:30	395	241		470	374	151
11:30-11:50	179	53		471	449	218
	Data Conv	DSP	RF, MW	Verification	Optics /Photo	Power Elect
12:00-12:20	37	60	349	323	64	124
12:20-12:40	57	138	359	448	188	303
12:40-13:00	231	343	398	261	432	388
13:00-13:20	282	237	105			
Lunch						
15:00-16:30	Poster	Poster		Poster	Poster	Poster
	Data Conv		Com & Wir	Multimedia	Embedded	
16:30-16:50	44		108	472	229	
16:50-17:10	170		291	473	352	
17:10-17:30	433		381	474		
17:30-17:50			430	475		
17:50-18:10				476		

Poster Session

Pos.	Paper ID	Pos.	Paper ID	Pos.	Paper ID
1	292	17	367	33	409
2	296	18	377	34	161
3	195	19	400	35	338
4	230	20	411	36	366
5	244	21	414	37	397
6	322	22	443	38	412
7	178	23	224	39	156
8	186	24	239	40	103
9	219	25	444	41	468
10	227	26	123	42	
11	314	27	329	43	
12	316	28	358	44	
13	334	29	402	45	
14	419	30	436	46	
15	423	31	348		
16	446	32	376		

Condesa I-A Room

Analog Circuits and Signal Processing 10:30 – 11:50

193 *Application of Active Current Mirrors to Improve the Speed of Analog Decoder Circuits*, Shahaboddin Moazzeni, Glenn E. R. Cowan, Concordia University, Canada

306 *CMOS Compatible High Voltage Compliant MESFET Based Analog IC Building Blocks*, Sungho Kim, William Lepkowski, Trevor J. Thornton, Bertan Bakkaloglu, Arizona State University, USA

395 *A 1-GS/s 6-bit Flash ADC in 90 nm CMOS*, Mohamed O. Shaker, Soumik Gosh, Magdy A. Bayoumi, University of Louisiana at Lafayette, USA

179 *Design Tradeoffs in a Triode Transconductor for Low Voltage Zero-IF Channel Select Filters*, John Richard Hizon, Esther Rodriguez-Villegas, Imperial College, United Kingdom

Data Converters 12:00 – 13:20

37 *$\Delta\Sigma$ ADCs with Second-Order Noise-Shaping Enhancement*, Yan Wang, Gabor C. Temes, Oregon State University, USA

57 *Excess Loop Delay Compensation Technique For Tunable Bandpass Delta Sigma Modulators*, M. Afifi, M. Keller, Y. Manoli, M. Ortmanns, University of Freiburg Freiburg, Germany, University of Ulm, Germany

231 *Double-Sampling $\Sigma\Delta$ Modulator with Relaxed Feedback Timing*, Weilun Shen, Gabor C. Temes, Oregon State University, USA

282 *A Fast Simulator for Pipelined A/D Converters*, Bibhu Datta Sahoo, Behzad Razavi, University of California, USA

Data Converters 16:30 – 17:50

44 *Track-and-Hold and Comparator for a 12.5GS/s, 8bit ADC*, Shohreh Ghetmiri, C. Andre T. Salama, University of Toronto, Canada

170 *The Design of Low-Power CFF Structure Second-Order Sigma-Delta Modulator*, Pin-Han Su, Herming Chiueh, National Chiao-Tung University, Taiwan

433 *A High Resolution Multibit $\Sigma\Delta$ DAC using Noise Shaping*, Swaran R. Singh, Vincent Gaudet, Kambiz Moez, University of Alberta, Canada

Condesa I-B Room

Digital Circuits 10:30 – 11:50

143 *The 90 nm Double-DICE Storage Element To Reduce Single-Event Upsets*, Mahta Haghi, Jeff Draper, University of Southern California, USA

165 *Switching-Voltage Detection and Compensation Circuits for Ultra-Low-Voltage CMOS Inverters*, Kei Matsumoto, Tetsuya Hirose, Yuji Osaki, Nobutaka Kuroki, Masahiro Numa, Kobe University, Japan

241 *A Comparative Analysis of Coarse-grain and Finegrain Power Gating for FPGA Lookup Tables*, Pradeep S. Nair, Santosh Koppa, Eugene B. John, University of Texas, USA

53 *A Novel CNTFET-Based Ternary Logic Gate Design*, Sheng Lin, Yong-Bin Kim, Fabrizio Lombardi, Northeastern University, USA

Digital Signal Processing 12:00 – 13:20

60 *DCGA Optimization of Lowpass FRM IIR Digital Filters Over CSD Multiplier Coefficient Space*, Syed Bokhari, Behrouz Nowrouzian, University of Alberta, Canada

138 *Low-Complexity Implementation of State-Space Structures in Linear DSP Synthesis*, S. Vijay, Arizona State University, USA

343 *Speech Enhancement Based on Adaptive Filter with Variable Step Size for Wideband and Periodic Noise*, Naoto Sasaoka, Koji Shimada, Shota Sonobe, Yoshio Itoh, Kensaku Fujii, Tottori University, Japan, University of Hyogo, Japan

237 *Residue-to-Decimal Converters for Moduli Sets with Common Factors*, Kazeem Alagbe Gbolagade, Sorin Dan Cotofana, Delft University of Technology, The Netherlands, University for Development Studies, Ghana

Condesa II Room

RF. Microwave Circuits 12:00 – 13:20

349 *A 1V Low Power 2~11 GHz Direct-Conversion Mixer for WiMAX System*, Yan-Cheng Pan, Zhi-Ming Lin, National Changhua University of Education, Taiwan

359 *A 1.6 GHz Switch Mode Power Amplifier with Continuous-Time Bandpass Delta-Sigma Modulator*, Manfred Berroth, Martin Schmidt, Stefan Heck, Alexander Braeckle, Markus Groezing, University of Stuttgart, Germany

398 *Multi-Standard Carrier Generator with CMOS Logic Divider*, Seonghan Ryu, Hannam University, Souht Korea

105 *On I/Q-Mismatch in Active Interference Cancellation Schemes*, Tobias D. Werth, Ralf Wunderlich, Stefan Heinen, RWTH Aachen University, Germany

Communications and Wireless Systems 16:30 – 17:50

108 *System Architecture of an RF-DAC Based Multistandard Transmitter*, Niklas Zimmermann, Björn Thorsten Thiel, Renato Negra, Stefan Heinen, RWTH Aachen University, Germany

291 *Mobility Support for Wireless Sensor Networks Simulations for Road Intersection Safety Applications*, Lars Hoehmann, Anton Kummert, University of Wuppertal, Germany

381 *Distributed Distribution-based Optimization for Sensor Fault Detection*, Peng Zhuang, Dan Wang, Yi Shang University of Missouri, USA

430 *Global System Approach to Validate a Wireless System even with a Multi-antennas Receiver Structure*, José Cruz Nuñez Pérez, Jacques Verdier, Guillaume Villemaud, Jean-Marie Gorce, CITEDI-Instituto Politécnico Nacional, México, Institut des Nanotechnologies de Lyon, France, Centre d'Innovation en Télécommunications et Intégration de Services, France

Ma. Beatriz Room

MEMS/NEMS & Nanoelectronics 10:30-11:50

355 *Design and Simulation of a RF MEMS Shunt Switch for Ka and V Bands and the Impact of Varying Its Geometrical Parameters*, Y. Mafinejad, A.Z. Kouzani, K. Mafinezhad, D. Azadi, Deakin University, Australia, Ferdowsi University, Iran

453 *Design and Fabrication of a Novel Microgripper Based on Electrostatic Actuation*, J. Varona, E. Saenz, S. Fiscal-Woodhouse, A. A. Hamoui, Universidad Panamericana-Bonaterrea, México, Snowbush IP, México, McGill University, Canada

470 *Nanoelectronic properties of Si and Ge: A semi-empirical approximation*, A. Miranda, F. A. Serrano, R. Vázquez-Medina, M. Cruz-Irisson, Instituto Politécnico Nacional, México

471 *Optical vibrational states of diamond nanocrystals*, F. A. Serrano, L. Niño de Rivera, V. Ponomaryov, M. Cruz-Irisson, Instituto Politécnico Nacional, México

Verification 12:00-13:20

323 *Optimal Trace Compaction with Property Preservation*, Yibin Chen, Sean Safarpour, Andreas Veneris, University of Toronto, Canada

448 *A Methodology to Compute the Statistical Fault Coverage of Small Delays due to Opens*, José L. García-Gervacio, Victor Champac, National Institute for Astrophysics, Optics and Electronics, México

261 *Logic Fault Test Simulation Environment for IP Core-Based Digital Systems*, Mansour H. Assaf, Leslie-Ann Moore, Sunil R. Das, Emil M. Petriu, Satyendra N. Biswas, Altaf Hossain, The University of Trinidad and Tobago, Trinidad y Tobago, University of Ottawa, Canada, Try University, USA, Georgia Southern University, USA

Multimedia Security and Content Protection 16:30-18:10

472 *Improvement in Spread Spectrum Watermarking through Convolutional Codes*, Mazay Jiménez-Salinas, Francisco García-Ugalde, Universidad Nacional Autónoma de México, México

473 *Watermarking Based Document Authentication in Script Format*, M. Gonzalez-Lee, C. Santiago-Avila, M. Nakano-Miyatake, H. Perez-Meana, National Polytechnic Institute, Mexico

474 *Adaptive JPEG Steganography Using Convolutional Codes and Synchronization Bits in DCT Domain*, Carlos Velasco, Mariko Nakano, Hector Perez, Raul Martinez, Kazuhiko Yamaguchi, National Polytechnic Institute, México, The University of Electro-Communications, Japan

475 *Network Forensics with Neurofuzzy Techniques*, Eleazar Aguirre Anaya, Mariko Nakano-Miyatake, Héctor Manuel Pérez Meana, Instituto Politécnico Nacional, México

476 *VideoWatermarking Scheme resistant to MPEG Compression*, Pedro A. Hernandez-Avalos, Claudia Feregrino-Urbe, Rene Cumplido, Jose Juan Garcia-Hernandez, National Institute for Astrophysics, Optics and Electronics, México

Ma. Mercedes Room

Neural Networks and Fuzzy Systems 10:30-11:50

263 *Learning and Recognition of Similar Temporal Sequences*, Robert H. Fujii, Taiichiro Hayashi University of Aizu, Japan

301 *An adaptive impedance matching approach based on fuzzy control*, E. Arroyo-Huerta, A. Díaz-Méndez, J.M. Ramírez-Cortés, J.C. Sánchez García, Instituto Nacional de Astrofísica Óptica y Electrónica, México, Instituto Politécnico Nacional, México

374 *An Approximation Method for Modeling a CMOS Bit-Level Product Cell*, Yesenia E. González-Navarro, Felipe Gómez-Castañeda, José A. Moreno-Cadenas, CINVESTAV-IPN, México

449 *AI Identification of New Hydro-Climate Models*, J. Szczupak, D. Sica, D. Silva, L. Pinto, L. Macedo, F. Savi, ENGENHO, Brazil

Optics and Photonics 12:00-13:20

64 *Optical Properties of Femtosecond Laser-Induced Periodic Surface Structures on Metals*, Anatoliy Y. Vorobyev, Vladimir S. Makin, Chunlei Guo University of Rochester, USA, The Research Institute for complex Testing of Optoelectronics Devices, Russia

188 *Chip-Scale Nanophotonic Chemical and Biological Sensors using CMOS Process*, Lincoln Bollschweiler, Alex English, R. Jacob Baker, Wan Kuang, Zi-Chang Chang, Ming-Hsiung Shih, William B. Knowlton, William L- Hughes, Jeunghoon Lee, Bernard Yurke, Nanyang Suh Cockerham, Vance C. Tyree, Boise State University, USA, National Chiao-Tung University, Taiwan, University of Southern California, USA

432 *Fault tolerance of a dynamic optically reconfigurable gate array with a one-time writable volume holographic memory*, Takayuk Mabuchi, Kenji Miyashiro, Minoru Watanabe, Akifumi Ogiwara, Shizuoka University, Japan, Takamatsu National College of Technology, Japan, Kobe City College of Technology, Japan

Embedded Systems and Electronics 16:30-17:50

229 *Hardware/Software Co-design Approach for a DCT-Based Watermarking Algorithm*, Y. Morita, E. Ayeh, O. B. Adamo, P. Guturu, University of North Texas, USA

352 *Yield Gain with Memory BISR – A Case Study*, Maddumage Karunaratne, Bejoy Oomann, University of Pittsburgh, USA, Genesys Testware Inc., USA

Ma. Fernanda Room

SoC and VLSI 10:30-11:50

434 *Ultra Low Leakage 90nm Content Addressable Memory Design for Wireless Sensor Network Applications*, Swaran R. Singh, Kambiz Moez, University of Alberta, Canada

91 *Assessment of CNTFET Based Circuit Performance and Robustness to PVT Variations*, Geunho Cho, Yong-Bin Kim, Fabrizio Lombardi, Northeastern University, USA

151 *An Efficient Methodology for Power Modeling and Simulation of Modern Cell-Based Microprocessors*, Ge Zhang, Weiwu Hu, Institute of Computing Technology, China

218 *A New SoC Video Ghost Canceller*, Jiaoying Huang, Yigang He, Yichuang Sun, Wenshan Zhao, Xi Zhu, Hunan University, China, University of Hertfordshire, United Kingdom

Power Electronics 12:00-13:20

124 *Modelling and Simulation of Power Electronic Converters Using the Component Connection Model*, K. Mino, J. Rico, E. , Universidad Michoacana de San Nicolás de Hidalgo, México

303 *A Capacitor-Free LDO Using a FD Si-MESFET Pass Transistor*, W. Lepkowski, S. J. Wilk, S. Kim, B. Bakalaglu, T.J. Thornton, Arizona State University, USA & SJT Micropower INC., USA

388 *Operation-Based Signal-Flow AC Analysis of Switching DC-DC Converters in CCM and DCM*, Dongwon Kwon, Gabriel A. Rincón-Mora, Georgia Institute of Technology, USA

Condesa III Room

Poster Session 15:00-16:30

292 *Embedded Hybrid DC-DC Converter with Improved Power Efficiency*, Kaushik Bhattacharyya, P. V. Ratna Kumar, Pradip Mandal, Indian Institute of Technology-Kharagpur, India

296 *Self-Biased Indicator Lamp Driver Circuits for High Reliability Applications*, Benjamin Amey, Texas Instruments Inc., USA

195 *A Wide-Band QPSK Modulator Using Branch-line coupler and MESFET Switches*, Muhammad Kashan Mobeen, Farhan Abdul Ghaffar, Sharjeel Qamar, Muhammad Hasan, SUPARCO, Pakistan

230 *A 3-5GHz Frequency Tunable Ultra Wideband LNA for OFDM Applications*, Fei Gong, Kin Fung Lam, Mohammed Ismail, Seok-Bae Park, Joanne De Groat, The Ohio State University, USA

244 *A CMOS Passive Mixer for Direct-Conversion Receivers*, Sherif A. Mohamed, Yiannos Manoli, Maurits Ortmanns, University of Freiburg, Germany, University of Ulm, Germany

322 *27.1GHz CMOS Distributed Voltage Controlled Oscillators With Body Bias for Frequency Tuning of 1.28GHz*, Kalyan Bhattacharyya, J. Mukherjee, M. Shojaei Baghini, Indian Institute of Technology, India

178 *A Novel Design Methodology to Optimize The Speed and Power of the CNTFET Circuits*, Young Bok Kim, Yong-Bin Kim, Fabrizio Lombardi, Northeastern University, USA

186 *Novel Reversible Division Hardware*, Noor Muhammed Nayeem, Md. Anan Hossain, Md. Mutasimul Haque, Laffa Jamal, Hafiz M. Hasan Babu, University of Dhaka, Bangladesh

219 *Design Automation Scheme for Wirelength Analysis of Resonant Clocking Technologies*, Vinayak Honkote, Baris Taskin, Drexel University, USA

227 *Piecewise Linear Delay Modeling of CMOS VLSI Circuits*, Jian Chang, Louis G. Johnson, Cheng Liu, Texas Instruments, Inc., USA, Oklahoma State University, USA

314 *Channel Charge Injection Analysis and Its Modeling in Z-Domain for Switched-Capacitor Integrators*, Pooya Torkzadeh, Mojtaba Atarodi, Sharif university of Technology, Iran, Mix Core Design

316 *Low Voltage Low Power Wide Range Fully Differential CMOS Four-Quadrant Analog Multiplier*, Soliman A. Mahmoud, German University in Cairo, Egypt

334 *A 0.13um CMOS Preamplifier for Low Level Signal Acquisition Systems*, Andreas Larsson, Sergio Solis, Intel Corporation, México

419 *Statistical Criteria of Design for Chaotic Analog Noise Generators*, R. Vázquez-Medina, A. Díaz-Méndez, M. Cruz-Irissou, J. L. Del-Rio-Correa, J. López-Hernández, National Polytechnic Institute, Mexico, National Institute of Astrophysics, Optic and Electronics & National Polytechnic Institute, Mexico, Metropolitan Autonomous University, México

423 *A Novel Divider using the Gilbert's cell with Floating Gate Feedback*, Fernando Lara-Villa, Fabian Yañez-Ortega, Ana L. Mota-Rodríguez, Ivan Padilla-Cantoya, Alejandro Diaz-Sanchez, Jose Miguel Rocha-Perez, Jesus Ezequiel Molinar-Solis, Instituto Nacional de Astrofisica, Optica y Electronica, Mexico, Universidad Autonoma del Estado de Mexico, México

446 *Mismatch Compensation in Winner-Take-All (WTA) Circuits*, Anshu Sarje, Pamela Abshire, University of Maryland, USA

367 *The Design of High Performance Elliptic Curve Cryptographic*, Jin-Hua Hong, Wei-Chung Wu, National University of Kaohsiung, Taiwan

377 *Handshaking Quasi-Adiabatic Logic*, Meng-Chou Chang, Chia-Chang Tsai, National Changhua University of Education, Taiwan

- 400 *Performance Evaluation of Multi-Operand Fast Decimal Adders*, Jeff Rebacz, Erdal Oruklu, Jafar Saniie, Illinois Institute of Technology, USA
- 411 *A Transmission Gate Flip-Flop Based on Dual-Threshold CMOS Techniques*, Linfeng Li, Jianping Hu, Ningbo University, China
- 414 *Low-Complexity Integrated Architecture of 4x4, 4x8, 8x4 and 8x8 Inverse Integer Transforms of VC-1*, Yi-Jung Wang, Chih Chi Chang, Guo Zua Wu, Oscar T.-C. Chen, Industrial Technology Research Institute, Taiwan, National Chung Cheng University, Taiwan
- 443 *Design Techniques of P-Type CMOS Circuits for Gate-Leakage Reduction in Deep Sub-micron ICs*, Weiqiang Zhang, Linfeng Li, Jianping Hu, Ningbo University, China
- 224 *Overflow Analysis in the Fixed-Point Implementation of the First-Order Goertzel Algorithm for Complex-Valued Input Sequences*, Modesto Medina-Melendrez, Miguel Arias-Estrada, Albertina Castro, Instituto Nacional en Astrofísica, Óptica y Electrónica, México
- 239 *Hybrid WHT-MRRNS Architectures for Fault Tolerant Adaptive Filters*, C. Radhakrishnan, W. K. Jenkins, The Pennsylvania State University, USA
- 444 *Multiple-Sound-Source Localization Scheme Based on Feedback-Architecture Source Separation*, Wen-Chih Wu, Oscar T.-C. Chen, WuFeng Institute of Technology, Taiwan, National Chung Cheng University, Taiwan
- 123 *Low-Power implementation of a 4x4 two-dimensional Discrete Pascal Transform*, Kundan Nepal, Branden Izumi, Bucknell University, USA,
- 329 *Energy adjustment RGB Images in Steganography Applications*, Blanca E. Carvajal-Gámez, Francisco J. Gallegos-Funes, José L. López-Bonilla, National Polytechnic Institute, Mexico
- 358 *Convolution Method for CCD Images Processing for DSO Astrophotography*, R. Suszynski, Koszalin University of Technology, Poland
- 402 *New Optimized Approach for Written Character Recognition Using Symlest Wavelet*, R. Munguia, K. Toscano, G. Sánchez, M. Nakano, National Polytechnic Institute, Mexico
- 436 *Automatic Ringing Artifact Detection in Restoring Blurred Face Images*, Wen-Chung Kao, Chih-Hsiang Chiu, Yueh-Yiing Yang, National Taiwan Normal University, Taiwan
- 348 *A 1-V 11.6-dBm IIP3 Up-Conversion Mixer for UWB Wireless System*, Wen-Shan Hxiao, Zhi-Ming Lin, National Changhua University of Education, Taiwan
- 376 *A Wide Frequency Range CMOS Active Inductor for UWB Bandpass Filters*, Md. Mahbub Reja, Kambiz Moez, Igor Filanovsky, University of Alberta, Canada
- 409 *A 10-GHz 0.88-mW Low-Phase-Noise CMOS VCO*, Jin-Rong Syu, Zhi-Ming Lin, National Changhua University of Education, Taiwan
- 161 *CMOS Distributed Paraphase Amplifier Employing Derivative Superposition Linearization for Wireless Communications*, Ziad El-Khatib, Leonard MacEachern, Samy A. Mahmoud, Carleton University, Canada
- 338 *Compact Model for Carbon Nanotubes Interconnects using Fourier Series Analysis*, Suraj Subash, Md Sajjad Rahaman, Masud H. Chowdhury, University of Illinois, USA
- 366 *Design and Implementation of a Low-power Cryptosystem SoC*, Jin-Hua Hong, Tun-Kai Yao, Liang-Jia Lue, National University of Kaohsiung, Taiwan
- 397 *Robust and High Performance Subthreshold Standard Cell Design*, S. Amarchinta, H. Kanitkar, D. Kudithipudi, Rochester Institute of Technology, USA
- 412 *Optimal Stall Insertion with Timing Skew Adjustment for Tunable LSIs*, Keisuke Inoue, Takayuki Obata, Yayumi Uehara, Mineo Kaneko, Japan Advanced Institute of Science and Technology, Japan
- 156 *Guiding Property Development with SAT-based Coverage Calculation*, Roberto Hoffmann, Paul Molitor, Martin-Luther-University Halle-Wittenberg, Germany
- 103 *Design of High-side Current Sense Amplifier with Ultra-wide ICMR*, Yang Yang, Wu Xiaobo, Zhejiang University, China
- 468 *Implementation and Analysis of the NLMS Algorithm on TMS320C6713 DSP*, C. A. Duran Villalobos, J. A. Tavares Reyes, J. C. Sanchez Garcia, National Polytechnic Institute, Mexico

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