Carrier separation and Vth measurements of W-La$_2$O$_3$ gated MOSFET structures after electrical stress

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Abstract: Using a W-La$_2$O$_3$ gated MOSFET structure, we report the effect of substrate and gate injection of electrons on the breakdown and electrical degradation characteristics of the gate stack. Using the carrier separation measurement technique, we are able to identify the major contributor to leakage current under various stress conditions. By stressing n- and p-channel MOSFETs with positive and negative gate voltages respectively, the degradation (Vth shift) after stress is obtained and compared to the polarity of the applied stress.

Keywords: La$_2$O$_3$, PMA, MOSFET, carrier separation, Vth shift

Classification: Electron devices

References


1 Introduction

With gate oxides (SiO$_2$) thinner than 2 nm, the increasing standby-power consumption due to the gate leakage current (Ig) becomes a critical issue in advanced CMOS devices. In order to reduce Ig, the dielectric film with a higher dielectric constant “k” and a relevant value of the barrier height is needed. Compared to other high-k materials, La$_2$O$_3$ has been considered as a potential candidate for the long-term replacement of SiO$_2$ because of its relatively high dielectric constant and band offsets to silicon [1, 2]. Moreover, since La$_2$O$_3$-gated transistors have presented good initial electrical characteristics [3], the research on this material should advance to the next stage where reliability data are collected and the understanding of the mechanisms for dielectric degradation and breakdown is identified in order to minimize the sources that lead to failure. In this report, we studied the impact of stress polarity on the breakdown and electrical degradation mechanisms of W-La$_2$O$_3$ gated MOSFETs.

2 Experiments

MOSFETs were fabricated on p-type and n-type (100) oriented silicon wafers following the gate last fabrication process [4] in order to avoid the high thermal budget during the activation of source/drain (S/D) regions. After S/D definition, La$_2$O$_3$ thin films were deposited on HF-last silicon surface by electron-beam evaporation using molecular-beam epitaxy MBE system.
(ANELVA I) at 300°C. The pressure in the chamber during the deposition was around $1 \times 10^{-7}$ Pa. This is followed by in-situ sputtering of tungsten (60 nm) at 150 W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of $\text{La}_2\text{O}_3$ surface to the environment. Because of this, the physical thickness of $\text{La}_2\text{O}_3$ cannot be measured by ellipsometry but by transmission electron microscopy. The metal deposition was done under an argon flow of 1.33 Pa. Patterning of the gate electrodes was done by reactive-ion etching using $\text{SF}_6$ gas with a 30 W power. Finally, post-metallization annealing (PMA) was done in $\text{N}_2$ ambient at 500°C for 5 min for both n and p-channel MOSFETs.

3 Results and discussion

When $\text{La}_2\text{O}_3$ is deposited on silicon, IL formation generally occurs at the $\text{La}_2\text{O}_3$/Si interface [5]. It is thus essential to consider a two-layer oxide stacked structure for the analysis and characterization of its reliability. By using a MOSFET structure, the total $I_g$ can be separated into its electron and hole components ($I_e$ and $I_h$ respectively) using the carrier separation method [6].

Schematic illustrations of the carrier separation measurement are shown in fig. 1 (A-B) for nMOSFET and pMOSFET structures, respectively. During substrate injection of electrons, a positive voltage is applied to the gate of an nMOSFET whereas a negative voltage is applied to the gate of a pMOSFET during gate injection so that the inversion condition can be reached for both structures in order to properly separate the contribution of electron and hole components on the gate leakage current. Fig. 1 (C-D) shows the evolution of both $I_e$ and $I_h$ components with respect to stressing time under substrate and gate injection conditions. From this figure, we can see that the dominant carrier for gate leakage current is electrons for substrate injection and holes for gate injection. Also, it is clearly seen that depending on the polarization of the gate voltage ($V_g$), two different oxide breakdown mechanisms will emerge. W/$\text{La}_2\text{O}_3$-IL stack stressed under substrate injection will produce a two-step breakdown behavior as compared to the one-single step breakdown found under gate injection. This difference might be related to the different dominant carrier for gate leakage current for each stress condition. The difference in the dominant carrier (electrons or holes) would have a different impact with respect to the required time for breakdown $t_{bd}$. A slightly longer $t_{bd}$ is found for substrate injection condition as compared to $t_{bd}$ for gate injection. This result suggests that injection of electrons into the oxide will produce relatively longer lifetimes before the breakdown of this $\text{La}_2\text{O}_3$-IL stack as compared to gate injection where most of the trapped carriers are holes. In order to get a clearer picture of the breakdown mechanisms, simplified energy band diagrams for both substrate and gate injection conditions are shown in fig. 2 (A-B).

During substrate injection (nMOSFET), a positive voltage is applied to the gate and both $I_e$ and $I_h$ are detected as shown in fig. 1 (C). The origin
Fig. 1. (A-B) Schematic illustrations of the carrier separation experiment for W-La$_2$O$_3$ gated nMOSFET and pMOSFET structures, respectively. (C) Evolution of gate leakage current with stressing time. I$_{\text{electron}}$ is the dominant component of the total Ig. A two-step breakdown behavior is observed. (D) Evolution of gate leakage current with stressing time. I$_{\text{hole}}$ is the dominant component of the total Ig. A one-step breakdown behavior is observed.

Fig. 2. (A) Energy band diagram for W-La$_2$O$_3$ gated nMOSFET under substrate injection stress. Only electrons flow through the oxide. (B) Energy band diagram for W-La$_2$O$_3$ gated pMOSFET under gate injection stress. Both electrons and hole flow simultaneously through the oxide.
of Ie comes from the tunneling of electrons through the La₂O₃-IL stack. The source for these electrons is the S/D regions that are connected once the channel is formed at sufficiently high positive gate voltages. Determining the origin of the hole current Ih however, is not so straightforward. Because of the metallic W gate, the possibility of cold or hot-hole injection from the gate is eliminated. The possible mechanisms that could explain the origin of Ih are now: 1) Anode-hole injection (AHI), 2) electron-hole (e-h) pair generation in the oxides’ bulk/interface via trap levels (TL), 3) tunneling of valence-band electrons from the substrate (leaving holes behind) into the La₂O₃ conduction band directly or via TL and, 4) generation–recombination currents after impact ionization of electrons. It is thought that hole generation via 1) AHI [7] (injected electrons from the substrate generate holes at the anode that can tunnel back into La₂O₃) and consequent 2) e-h pair generation via TL within the bulk/interfaces of La₂O₃ are more plausible mechanisms for the origin of Ih since the oxide tends to develop a high density of TL because of its highly defective nature after deposition [8]. During the application of a continuous electrical stress, more traps or defects within the insulator are created [9]. The two-step nature of the breakdown event during stress is interpreted as precedent breakdown of the IL, followed by the breakdown of the La₂O₃ layer.

In the case of gate injection (pMOSFET), the first and only breakdown event takes place at a slightly shorter t_{bd}. A shorter t_{bd} would come by considering a heavier mass for holes that consequently would make more easy for these carriers to be trapped into the oxide during the stress. The sudden current jumps for both electrons and holes occur simultaneously at t_{bd}, see fig. 1 (D), and the breakdown process is considered to start with the simultaneous breakdown of both La₂O₃ and the IL layers. It is thought that the “direction” for the propagation of breakdown is strongly dependent on the polarity of the stress applied. The breakdown propagation would be from cathode towards the anode direction, in other words, dielectric breakdown would occur along the electron current direction for both injection conditions. Interestingly, the post-breakdown current levels for substrate injection are smaller than those for gate injection, fig. 1 (C-D). This is explained by considering different sizes for the leakage spots after breakdown. It is thought that the total area size of the breakdown spot in gate injection is larger than that after substrate injection. For La₂O₃, it is not clear yet whether a single big-size spot or multiple smaller-size spots are responsible for different post-breakdown Ig levels; Hf-based oxides however, have reported [10] direct evidence of the generation of a single big-size breakdown spot after breakdown during gate injection conditions.

Finally, the influence of substrate and gate injection stress conditions on the electrical characteristics of n and p-channel MOSFET structures is shown in fig. 3 (A-B). Here, the shift in threshold voltage Vth is plotted against the density of injected charge Qinj. Substrate injection conditions will produce a monotonous increase in Vth shift after stress whereas gate injection will produce smaller Vth shift at the same density of injected charge. Nonetheless,
Fig. 3. (A) Vth shift for a W/La₂O₃-IL stacked nMOSFET structure after substrate injection stress. A small but progressive Vth shift after stress is found. (B) Vth shift for a W/La₂O₃-IL stacked pMOSFET structure after gate injection stress. Vth hardly shifts after the first injection of charge.

gate injection produces a huge shift in Vth (tenths of millivolt) after the first stressing measurement which is in contrast to the smaller but progressive Vth shifts (few millivolts) produced by substrate injection. Because holes are the major carrier contributors to leakage current during gate injection and since they have a heavier mass than electrons during conduction, it is thought that the density of available sites for the trapping of holes during stress is rapidly filled and saturated after the first injected charges are trapped.

4 Summary

The effect of electron and hole currents on the breakdown and electrical degradation of the W-La₂O₃ gate stack was investigated by carrier separation and Vth shift measurements on both n- and p-channel MOSFETs. The dominant carrier for the leakage current is strongly dependent on the polarity of the applied stress and this has profound effects on the breakdown characteristics of the oxide layers. Under substrate injection, electrons from the channel are the main contributors to Iₓ and a two-step breakdown behavior is observed. It is thought that the first-breakdown event corresponds to the breakdown of the IL. For gate injection, holes become the main contributors to Iₓ and a one-step breakdown behavior is observed. By comparing the post-breakdown gate leakage currents for both substrate and gate injection conditions, it is thought that the area size of the breakdown spot after gate injection is larger than that after substrate injection, thus suggesting that the stress-induced damage is also strongly polarity dependent. Finally, the Vth shift dependence on Qinj is also polarity dependent, with gate injection producing the larger shifts in Vth even after an initially small density of
injected charge.

5 Acknowledgments

This work was partially supported by the Semiconductor Technology Academic Research Center (STARC) and Special Coordination Funds for Promoting Science and Technology by Ministry of Education, Culture, Sports, Science and Technology, Japan.