

DESIGN STRATEGIES FOR OPTICAL COMMUNICATION RECEIVER FRONT-ENDS IN CMOS TECHNOLOGY

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Abstract

Traditionally, optical fiber communications have been exploited for shared long-haul communication links. In cases like this, the high cost of transmitter and receiver, fabricated using GaAs or InP technology to achieve the standard requirements, is compensated by the huge number of users. However, the ever-increasing amounts of data transmitted over short-distances (50m) mandate the cost efficiency of the system. For such an application, the economic viability requires the use of the low-cost technologies for both microelectronic and optical components. The electronic front-end can be fabricated using a standard CMOS technology. For the optical channel polymethyl-methacrylate or 'plastic' optical fibers (POF) is a cost-effective choice.

In short-reach communications, standard 1mm step-index plastic optical fiber (SI-POF) offers certain advantages over copper cabling: (i) total immunity to EMI, (ii) possibility of being deployed in power-line ducts and (iii) thinner cables. Compared to glass optical fiber, it presents: (i) much simpler optoelectronic connections, (ii) possibility of RCLED or VCSEL based light emitters and (iii) mainly a reduction of overall cost. Recently, 1mm SI-POF has been standardized as A4a.2 and is starting to be used massively in the automotive sector (25Mbps) and industrial automation (100Mbps). Also, home networking is commencing; while the required bit rate in fiber-to-the-home (FTTH) applications is 100Mbps over 50m, the goal set by some telecom operators for home networking is to achieve speeds of several Gbps. However, receivers with adaptive gain and equalization are mandatory to compensate for the band-limited frequency response due to the large photodiode required and to the frequency response of the fiber. Typical loss at 650nm is of 0.14dB/m and the length-bandwidth dependency is around 40MHz·100m.

This talk presents a design methodology for full integrated front-end receiver implementation in nano CMOS technology for FTTH applications at Gbps transmission speed on SI-POF. The receiver architecture contains: photodetector (PD), transimpedance preamplifier (TIA), equalizer and postamplifier. Different TIAs are described and the proposed topology is designed in detail. Continuous-time equalizers have been chosen instead of more sophisticated DSP based approaches because they work independently of the clock recovery circuit and are suitable for low-power and high-speed applications. The postamplifier is able to provide a constant level output thanks to its double control loop of gain and dc offset. The combination of pre and postamplifier with gain control ensures a proper signal quality at the input of the equalizer and at the output of the receiver over a wide input dynamic range.

Experimental measurements will show an error-free sensitivity below -16dBm for 1.25Gbps with power consumption below 110mW. Currently, we are working towards a prototype with up to 3.125Gbps, which targets 10Gbps for Ethernet 10GBase-LX4 standard.