

**Title: Architecture-level Thermal Modeling and Simulation for
Multi-Core Chip Design**

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Abstract:

As CMOS technology is scaled into the nanometer region, the power density of high-performance microprocessors has increased drastically. The exponential power density increase will in turn lead to average chip temperature to rise rapidly. Higher temperature has significant adverse impacts on chip packing cost, performance and reliability. Excessive on-chip temperature leads to slower transistor speed, more leakage power consumption, higher interconnect resistance, and reduced reliability. Chip-multiprocessing techniques, where multiple CPU-cores and caches are integrated into a single chip, provide a viable solution to the temperature/power problems. But managing thermal effects in the design of multi-core microprocessors still remains a challenging problem.

In this talk, I will present the novel thermal modeling and analysis techniques at the multi-core architecture level for potential run-time dynamic thermal management and designing more thermal-efficient multi-core microprocessors. I will first present moment matching based fast thermal analysis algorithm, called TMM and compare it with HotSpot-based thermal analysis method. I then present several parameterized behavioral thermal modeling techniques at MSLAB@UCR for multi-core microprocessor designs. The first method applies the function-of-pencil and the response surface model methods to build thermal models, which allows variable design parameters such as thermal conductivities of sink materials, locations of thermal sensors, etc for efficient thermal-aware design exploration. The second approach is based on the subspace identification method, which allows general power and temperature waveforms to build the thermal models. I also present some latest developments on composable thermal modeling research at UCR. A number of examples based on Intel quad-core microprocessors will be presented.