

## Bio of Dr. Sheldon X.-D. Tan

Dr. Tan is an Associate Professor in the Department of Electrical Engineering, University of California at Riverside. He received his B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China in 1992 and 1995, respectively and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, in 1999.

Dr. Tan research interests include several aspects of design automation for VLSI integrated circuits – modeling and simulation of analog/RF/mixed-signal VLSI circuits, high performance power and clock distribution network simulation and design, signal integrity, power modeling, architecture-level thermal modeling and simulation, thermal optimization in nanometer VLSI design, and embedded system designs based on FPGA platforms. He has published 2 books, over 150 peer-reviewed journal and conference papers and gave about 50 invited presentations, tutorials and short courses at conferences and workshops.

Dr. Tan received NSF CAREER Award in 2004, and the Outstanding Oversea Investigator Collaboration Award from the NSF of China in 2008. He received the Best Paper Award Nomination from 2009 Design Automation Conference, the Best Paper Award from 2007 IEEE International Conference on Computer Design (ICCD'07), the Best Paper Award Nomination from 2005 Design Automation Conference, the Best Paper Award from 1999 Design Automation Conference. He received the UC Regent's Faculty Fellowship in 2004 and 2006 and COR (committee on Research) Research Fellowship from UCR in 2008. He also co-authored book "Symbolic Analysis and Reduction of VLSI Circuits" by Springer/Kluwer 2005 and "Advanced Model Order Reduction Techniques for VLSI Designs", by Cambridge University Press 2007. Dr. Tan now is serving as an Associate Editor for ACM Transaction on Design Automation of Electronic Systems (TODAE), Integration, The VLSI Journal, and Journal of VLSI Design.