Exploring MOSFET threshold voltage extraction methods

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Distinguished Lecture Program

1. Introduction:

The threshold voltage is a fundamental parameter for reliability assessment.

Our 2002 review article [OR02] has 133 citations in Scopus (see tables from 26/Aug/2013).

Since then there have been many additional publications about threshold voltage extraction methods.

We have just updated our review paper [OR13].

Both review articles have been in the list of the top 25 hottest articles in *Microelectronics and Reliability*.

We are now updating both papers.

YEAR	CITES
2003	2
2004	2
2005	4
2006	10
2007	13
2008	11
2009	20
2010	15
2011	21
2012	23
2013	12

COUNTRY	CITES
United States	33
China	22
France	18
Venezuela	15
Brazil	12
Taiwan	9
India	8
Japan	8
South Korea	7
Germany	5
Greece	5
Belgium	4
Mexico	4
Singapore	4
Ukraine	4
United Kingdom	4
Bangladesh	3
Israel	3
Italy	3
Hong Kong	2
Ireland	2
Malaysia	2
Portugal	2
Sweden	1
Serbia	1
Spain	1
Lebanon	1
Tunisia	1
Turkey	1

[OR02] A. Ortiz-Conde, F. J. García Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", Microelectronics Reliability, vol. 42 , pp. 583-596, May 2002.

[OR13] A. Ortiz-Conde, F.J. García-Sánchez, J. Muci, A. Terán Barrios, J.J. Liou,, C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods", Microelectronics Reliability 53 (1) , pp. 90-104, 2013.

Our previous article [OR02] reviewed 14 methods to extract V_T

For crystalline MOSFETs biased in the linear region:

1) Constant-current (CC)
2) Linear extrapolation (LE)
3) Transconductance Linear extrapolation (GMLE) from Tsuno in 1998.
4) Second Derivative (SD) from Wong in 1987.
5) Current-to-square-root-Transconductance Ratio (CsrTR $=I_D/g_m^{0.5}$) by independent work by Jain and and by Ghibaudo in 1988.
6) Transition (based on integration) and it was developed by us in 2000.
7) Integral (based on integration) and it was developed by us in 1997.
8) Corsi (based on an auxiliary function) published in 1993.
9) Second Derivative logarithmic (SDL) proposed by Aoyama in 1995.
10) Linear cofactor difference operator (LCDO) developed by He in 2002.
11) Non-linear optimization

For crystalline MOSFETs biased in the saturation region:

1) Linear extrapolation (LE)
2) G_1 function developed by us in 2001

For non-crystalline MOSFETs biased in the saturation region:

1) H function developed by us in 2001

[OR02] A. Ortiz-Conde, F. J. García Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods“, Microelectronics Reliability, vol. 42 , pp. 583-596, May 2002.

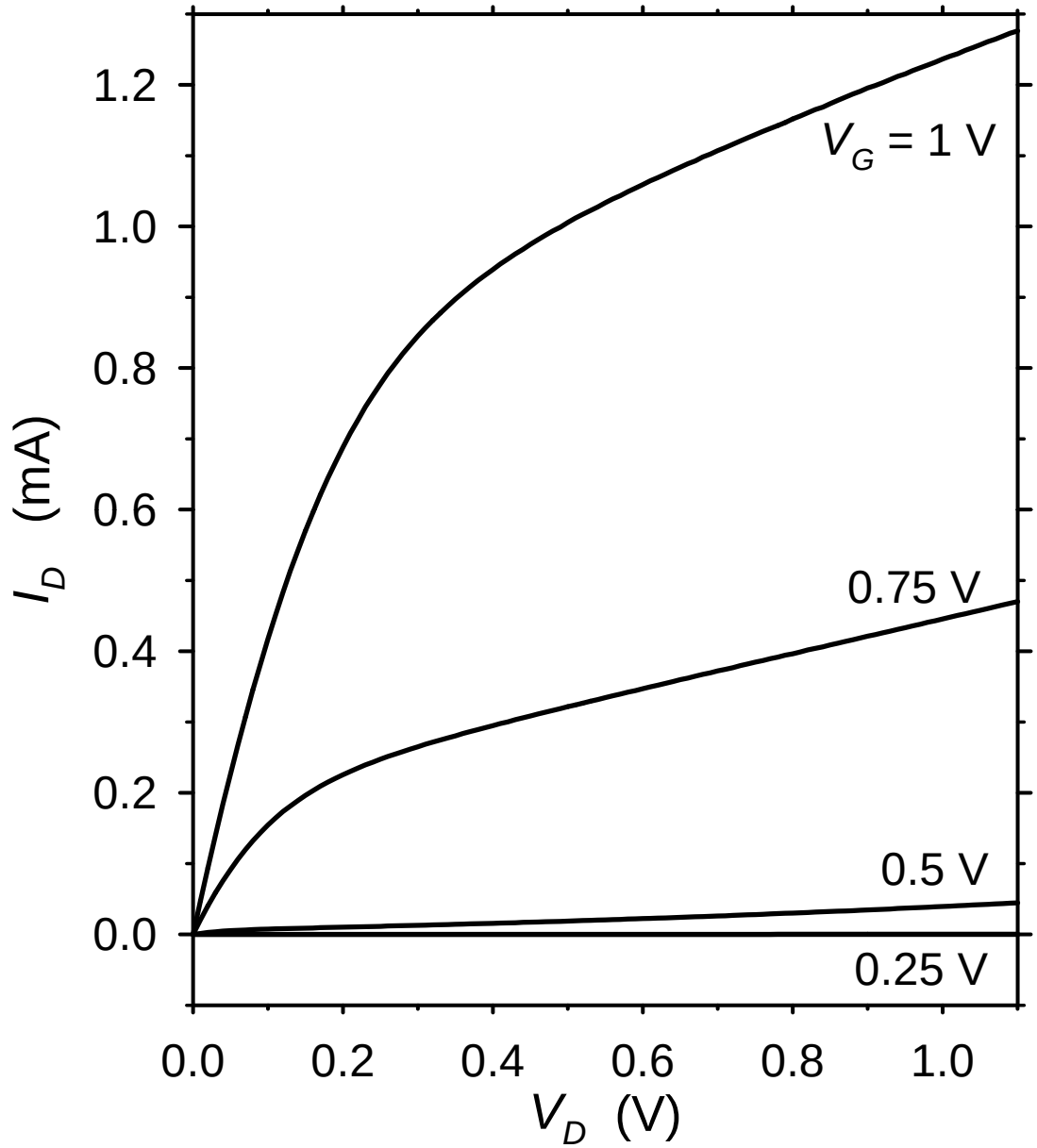
Boudinet reviewed [BO09] eight V_T extraction methods

1) Linear extrapolation (LE)
2) Transconductance Linear extrapolation (GMLE) from Tsuno in 1998.
3) Second Derivative (SD) from Wong in 1987.
4) Current-to-square-root-of-Transconductance Ratio (CsrTR $=I_D/g_m^{0.5}$) by independent work by Jain and and by Ghibaudo in 1988.
5) Corsi (based on an auxiliary function) published in 1993.
6) Second Derivative logarithmic (SDL) proposed by Aoyama in 1995.
7) Linear cofactor difference operator (LCDO) developed by He in 2002.
8) Transition (based on integration) and it was developed by García Sánchez et al in 2000.

They recommended: SD, CsrTR, and LCDO methods.

[BO09] D. Boudinet, G. Le Blevennec, C. Serbutoviez, J.-M. Verilhac, H. Yan, and G. Horowitz, "Contact resistance and threshold voltage extraction in n-channel organic thin film transistors on plastic substrates", J. Applied Physics 105, 084510, 2009.

To compare the different methods, we will apply them to measured characteristics [HO12,OR13] of a state-of-the art MOSFET with:
***W*=5 μm,**
***L*=65 nm,**
t_{ox}= 2.6 nm.



[HO12] Ching-Sung Ho, Powerchip Semicond. Corp., Hsinchu Science-Based Industrial Park, Hsinchu, Taiwan, 2012.

[OR13] A. Ortiz-Conde, F.J. García-Sánchez, J. Muci, A. Terán Barrios, J.J. Liou,, C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods", Microelectronics Reliability 53 (1) , pp. 90-104, 2013.

2.1. Constant-Current (CC) method

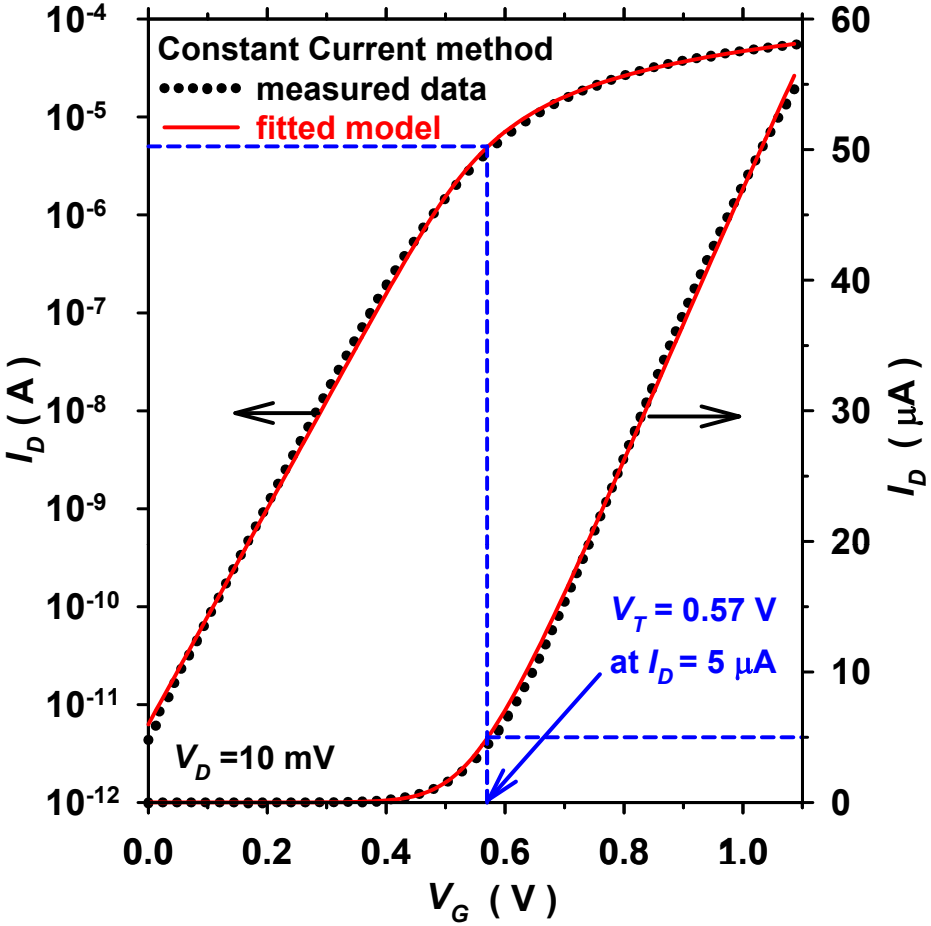
Threshold voltage is defined as the value of gate voltage corresponding to a given (arbitrary) constant drain current.

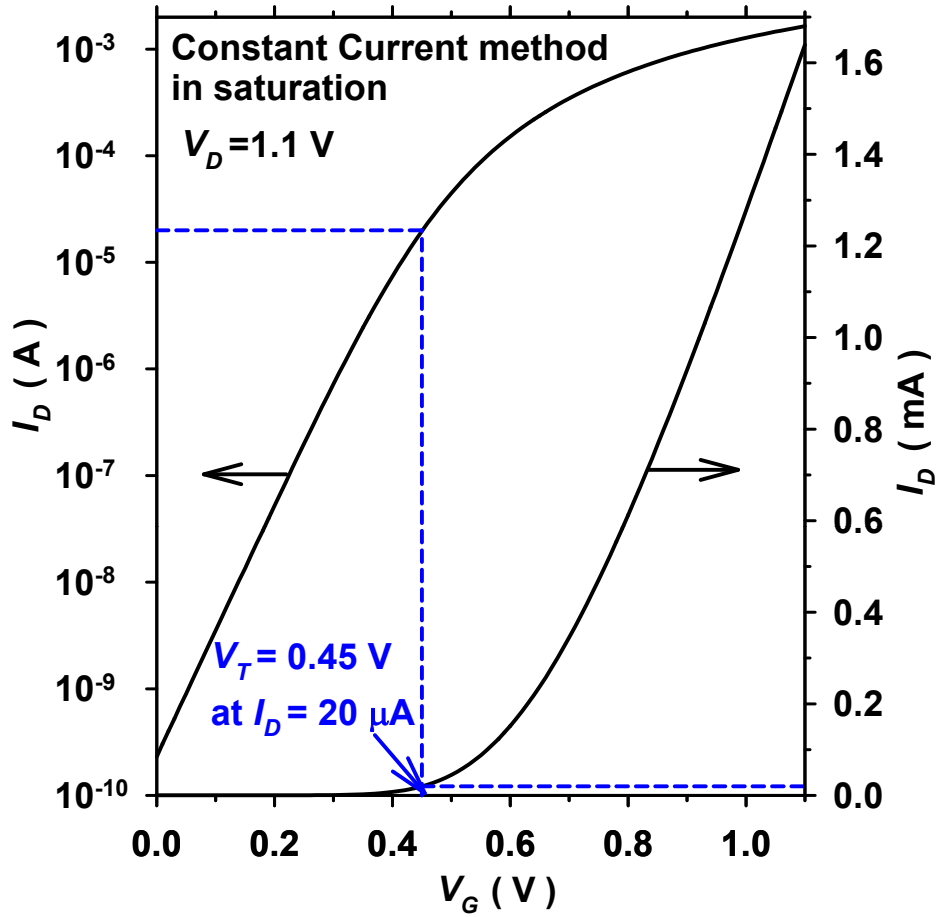
Tsuno proposed [TS99] that this constant drain current be (W_m/L_m) x 10^{-7} where W_m and L_m are the mask channel width and length, respectively.

Bazigos recently proposed [BA11] that this constant drain current should be dependent on drain voltage in order to obtain a consistent threshold voltage in the saturation region.

[TS99] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. , Physically-based threshold voltage determination for MOSFET's of all gate lengths. IEEE Transactions on Electron Devices 1999; 46: 1429 –1434.

[BA11] Bazigos, A., Bucher, M., Assenmacher, J., Decker, S., Grabinski, W., Papananos, Y. "An adjusted constant-current method to determine saturated and linear mode threshold voltage of MOSFETs", IEEE Transactions on Electron Devices 58 (11) , art. no. 6003772 , pp. 3751-3758, 2011.



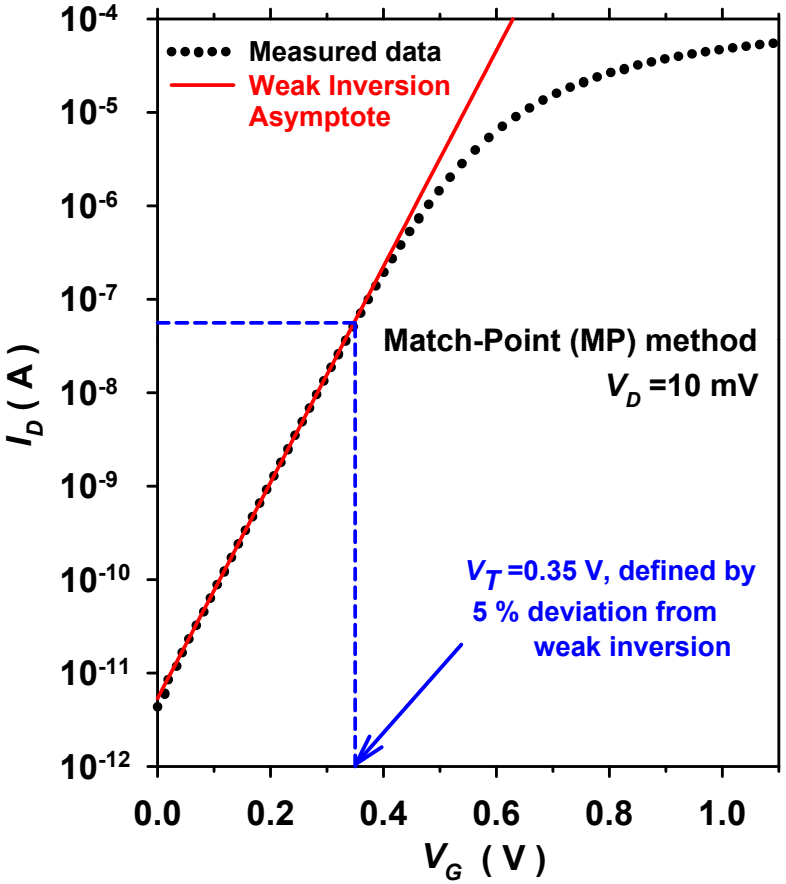


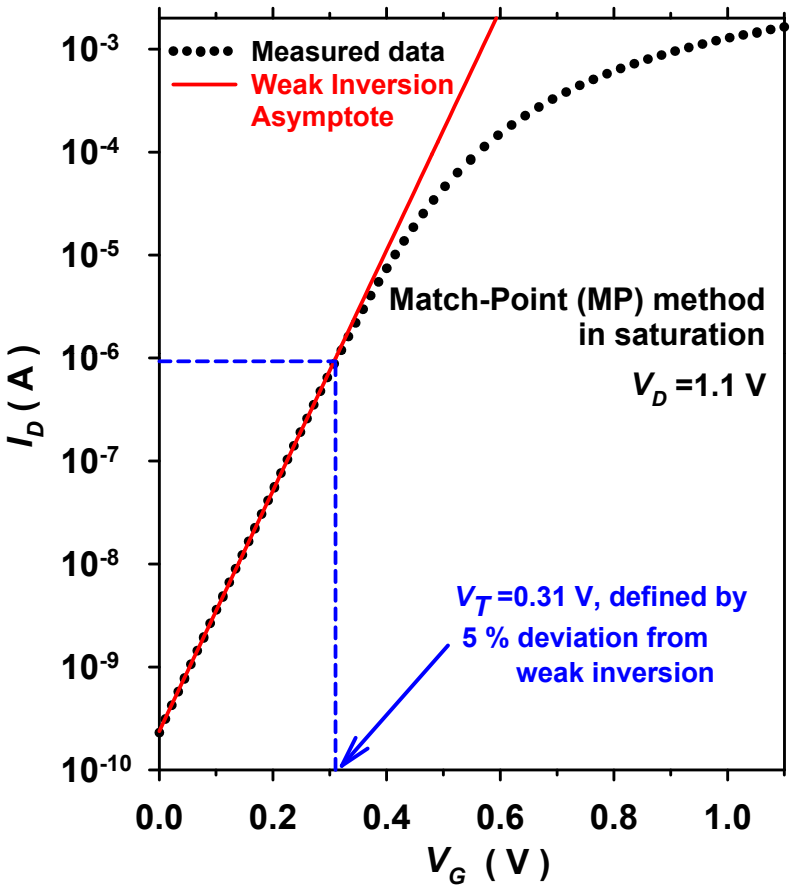
Semi-empirical approximation for small V_D [OR13]:

$$I_D = \frac{I_o}{(1+\theta V_{GS})} W\left[K\,(1+\theta V_{GS})\,e^{\frac{V_{GS}}{n v_{th}}}\right] \Rightarrow V_{GS} = \frac{n v_{th}\ln(I_D) + \left(\frac{n v_{th}}{I_o}\right) I_D - n v_{th}\ln(K I_o)}{1-\left(\frac{n v_{th}\theta}{I_o}\right) I_D}$$

2.2. Match-Point (MP) method

The MP method [KA90] establishes that V_T occurs at the gate voltage for which the exponential extrapolation of subthreshold current deviates by 5% from the measured current.





It overemphasizes weak inversion and neglects strong inversion.

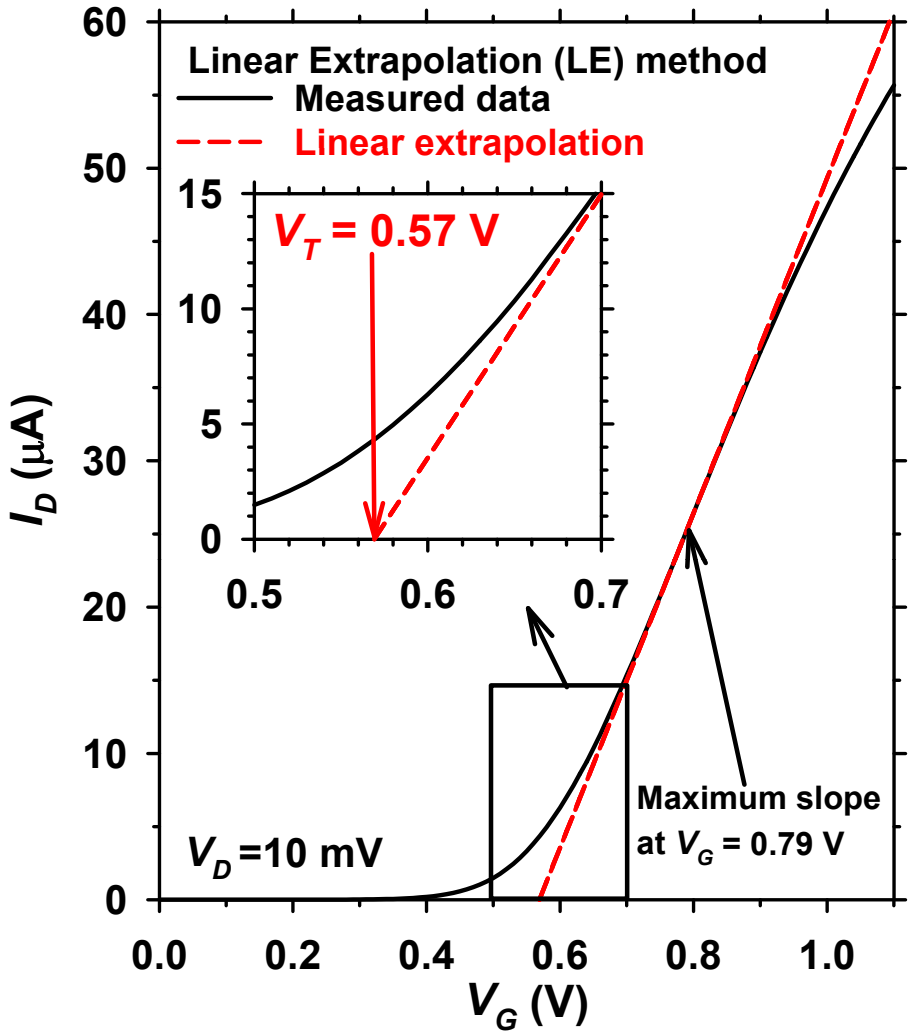
[KA90] B. El-Kareh, W. R. Tonti, and S. L. Titcomb, "A submicron MOSFET parameter extraction technique," IBM J. Res. Develop., vol. 34, pp. 243-249, 1990.

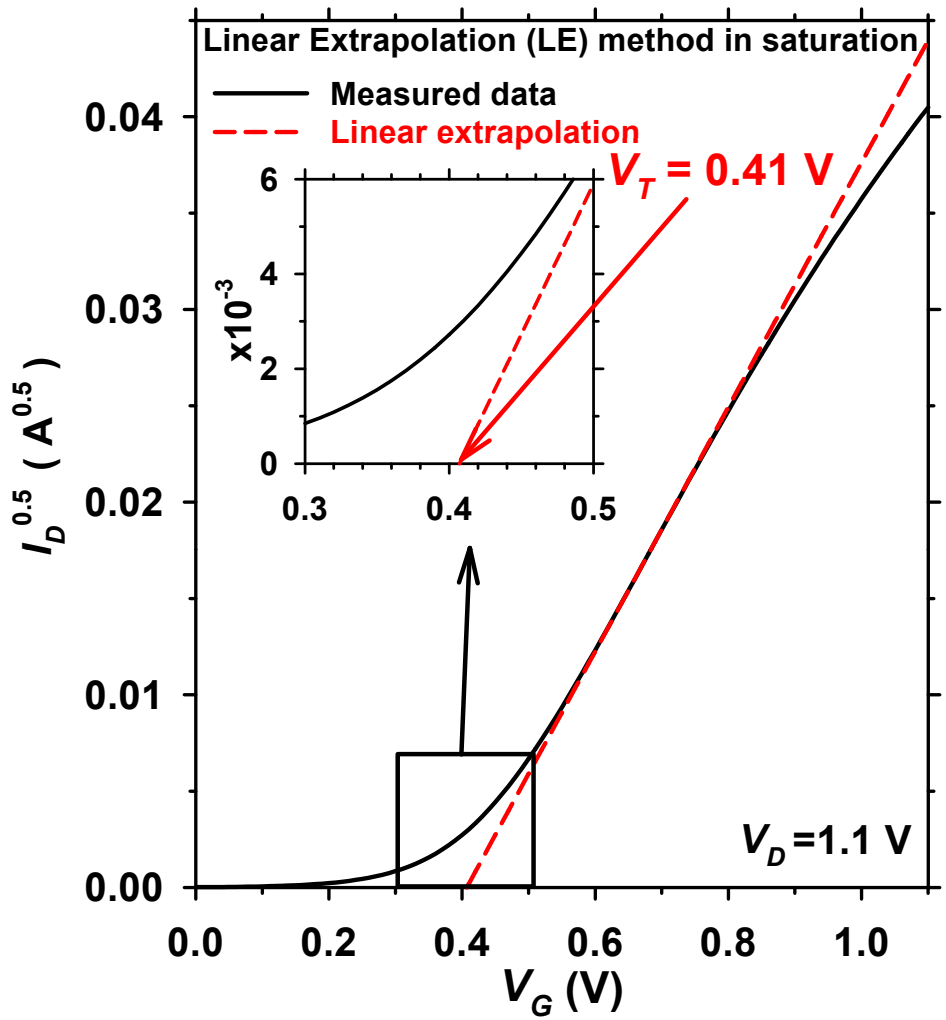
2.3. Linear Extrapolation (LE) method

***For the linear region*: It consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the I_D-V_G curve linear extrapolation at its maximum first derivative point.**

Then, the value of V_T is often calculated by subtracting $V_D / 2$ from the resulting gate-voltage axis intercept.

***For the saturation region*: The LE method, is similar to that in the linear region but it uses the $I_{Dsat}^{0.5}$-V_G characteristics instead.**


Linear Extrapolation (LE) method
Measured data
Linear extrapolation
V_T = 0.57 V
Maximum slope
at V_G = 0.79 V
V_D =10 mV
I_D (μA)
V_G (V)


Linear Extrapolation (LE) method in saturation
Measured data
Linear extrapolation
V_T = 0.41 V
x10^{-3}
V_D =1.1 V
$I_D^{0.5}$ ($A^{0.5}$)
V_G (V)

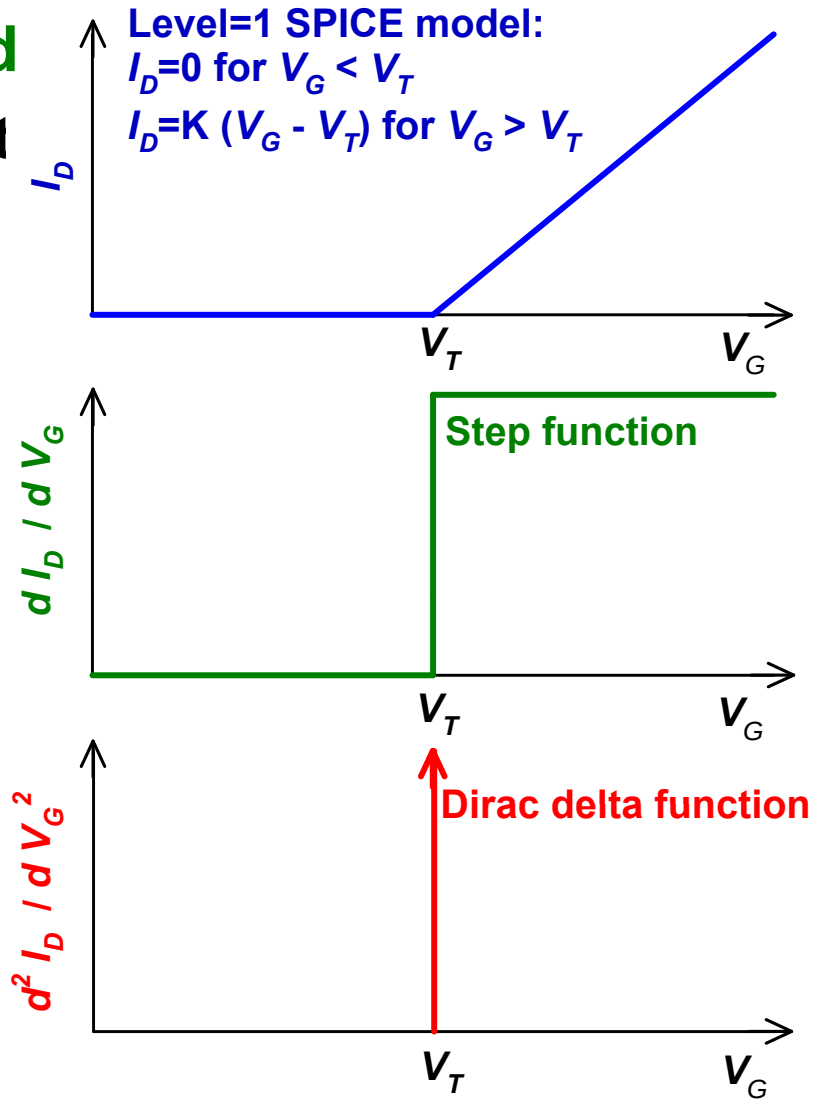
2.4. Second-derivative (SD) method

It determines V_T as the gate voltage at which the second derivative of the current (i.e., d^2I_D/dV_G^2) is maximum [WO87].

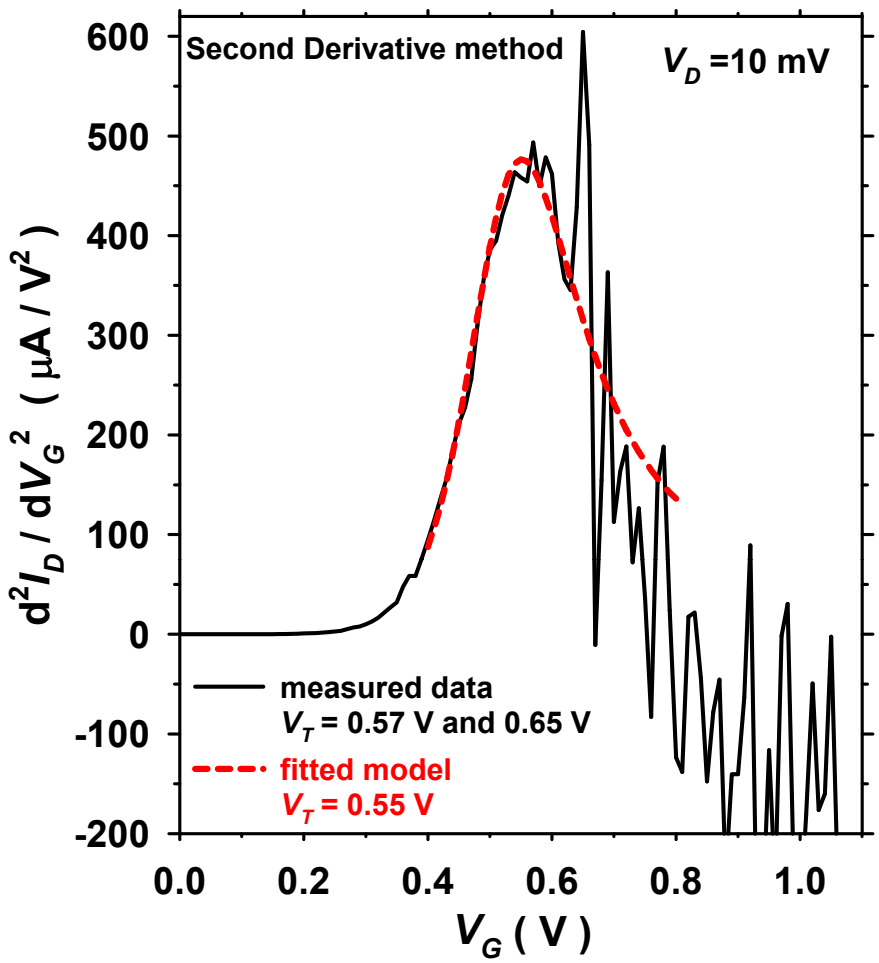
The origin of this method can be understood by analyzing Level=1 SPICE model, where I_D=0 for $V_G < V_T$ and I_D is proportional to V_G for $V_G > V_T$.

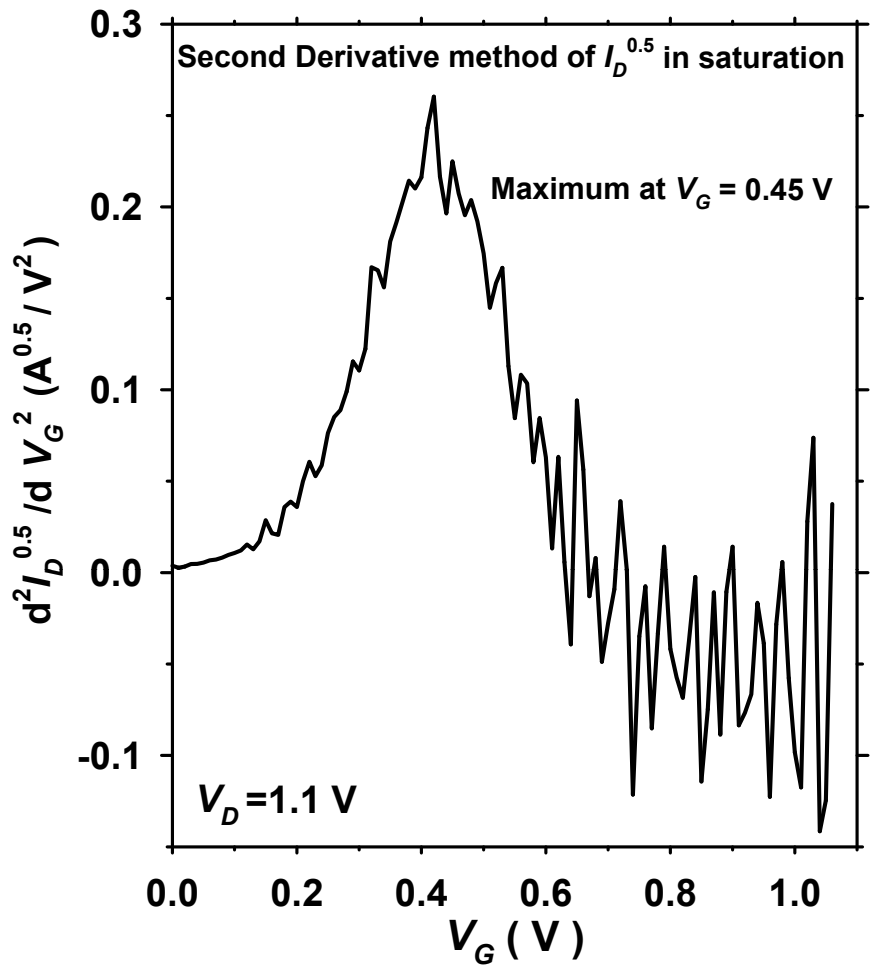
Using above assumption, dI_D/dV_G becomes a step function, and d^2I_D/dV_G^2 is a Dirac delta function.

For a real device d^2I_D/dV_G^2 will exhibit a maximum at $V_G = V_T$.



[WO87] Wong HS, White MH, Krutsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's. Solid-St.Electron. 1987; 30: 953.



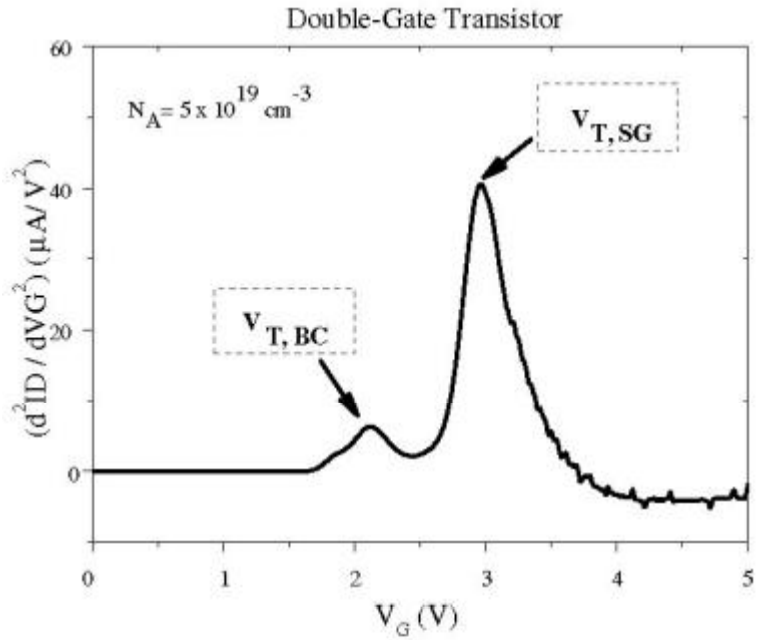


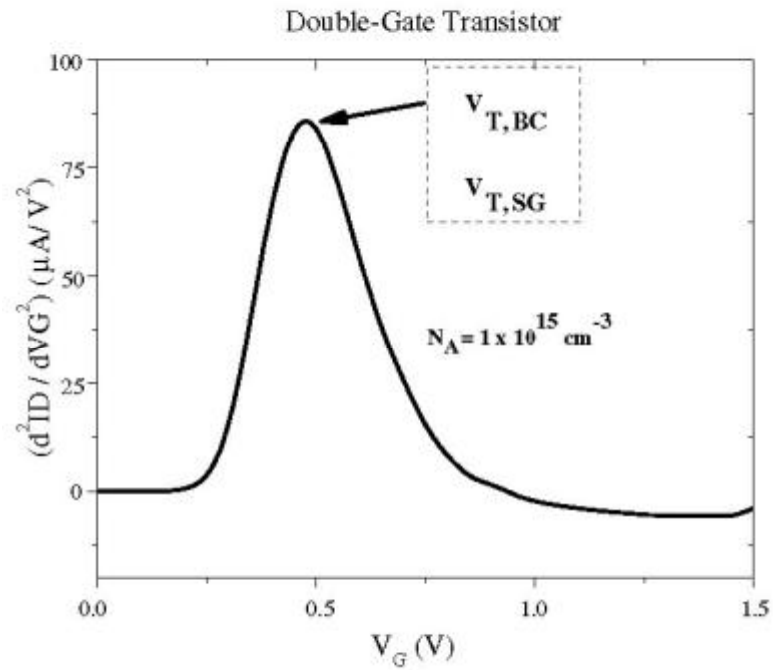
Measurement noise can be reduced by numerical smoothing techniques, or by fitting the semi empirical model described previously to the measured data, and thereafter performing the numerical derivatives.

Andrade and Martino [AN08], using the SD method, observe various V_T for SOI MuGFETs

For DG transistors, one or two V_T can be observed [AN08], depending on the channel doping concentration.

For triple-gate and quadruple-gate it is possible to observe up to four V_T due to corner effects and different doping concentration between the top and bottom of the Fin.





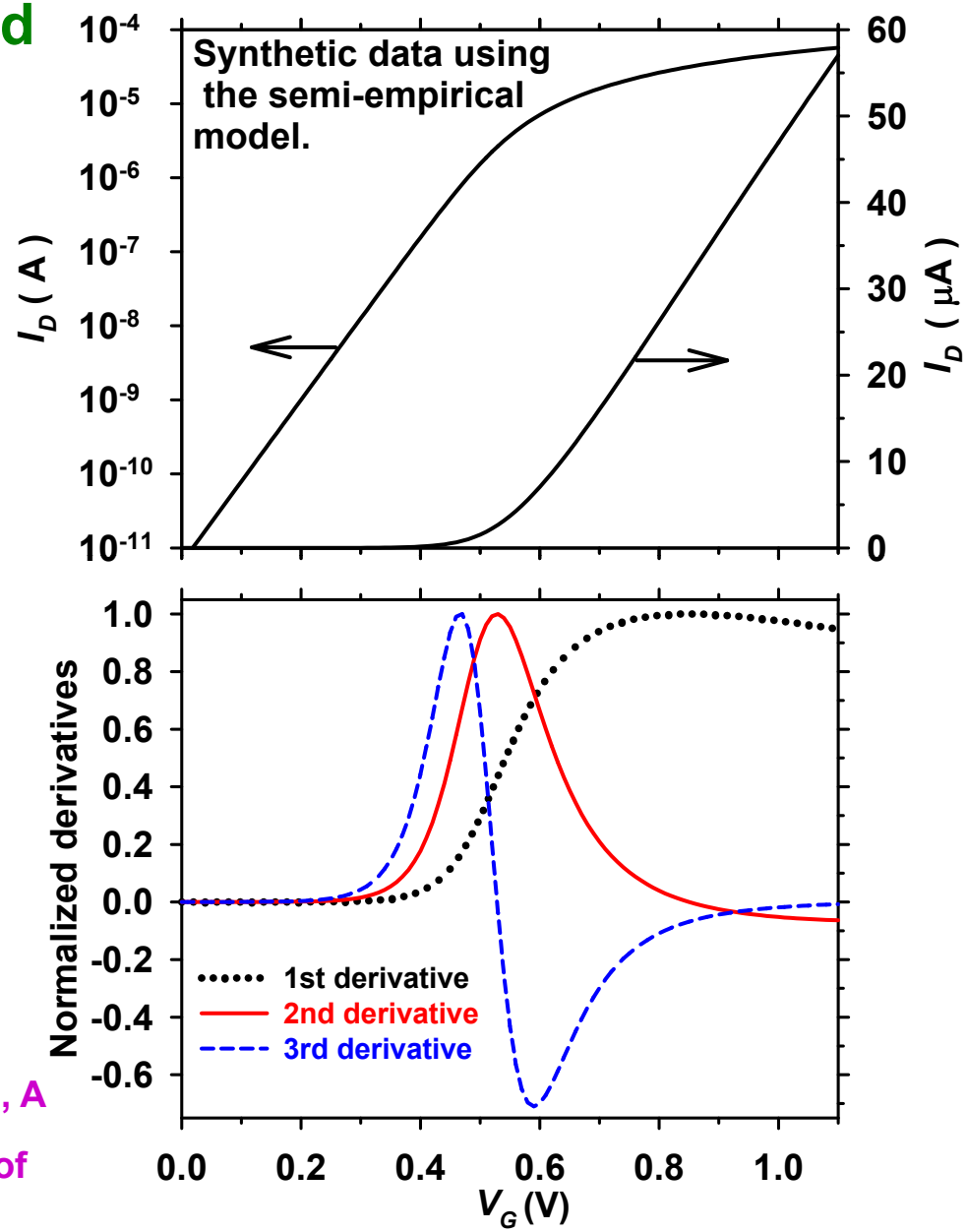
[AN08] M. G. Caño de Andrade, J. A. Martino, "Threshold voltages of SOI MuGFETs", Solid-State Electronics, 52 (2008), 1877–1883.

2.5. Third-derivative (TD) method

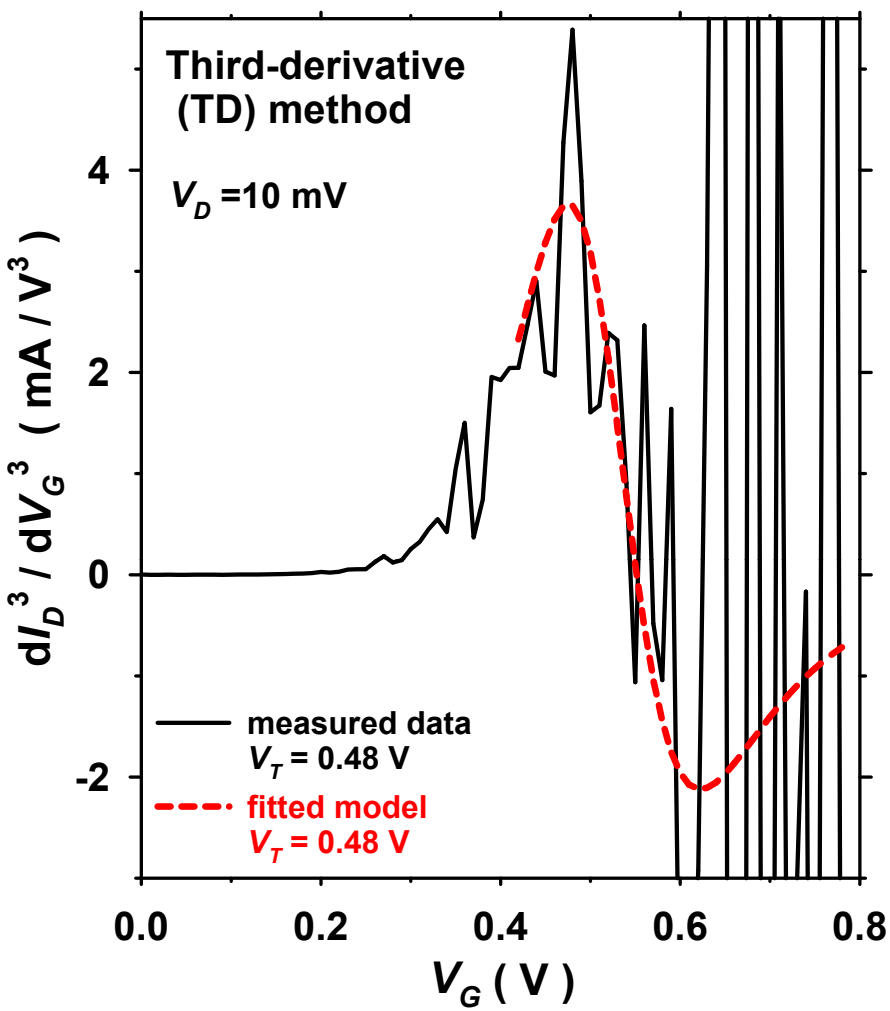
The TD method [WO01] determines V_T as the gate voltage at which the third derivative of the current (i.e., d^3I_D/dV_G^3) is maximum.

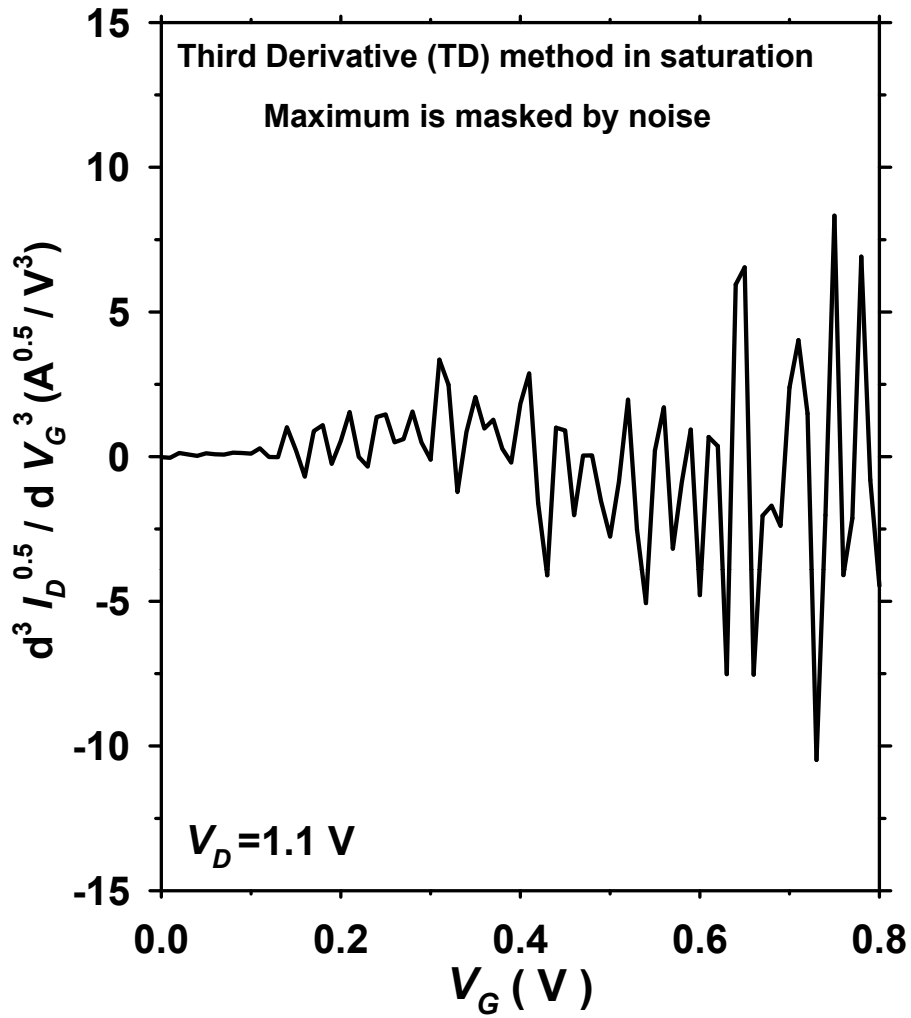
The maximum and minimum of d^3I_D/dV_G^3 are always located to the left and right of the maximum of d^2I_D/dV_G^2, as is illustrated in the figure.

Therefore, **this method is inconsistent with the second derivative method**.



[WO01] Wong, J.S. , Ma, J.G., Yeo, K.S., Do, M.A., A new approach for the extraction of threshold voltage for MOSFETs, Modeling and Simulation of Microsystems (MSM), pp. 534-537, 2001.





The Third-derivative (TD) method suffers from severe problems from experimental noisy data. The measurement noise can be reduced with numerical smoothing techniques or by fitting the semi empirical model described previously to the measured data, and thereafter performing the numerical derivatives.

2.6. Current-to-square-root-Transconductance Ratio (CsrTR) method

For strong inversion [JA88; GH88; FI95; SU10;JO11] :

$$CsrTR \equiv \frac{I_D}{\sqrt{g_m}} \equiv \frac{I_D}{\sqrt{dI_D/dV_G}} = s^{-1/2}\left(V_G - V_T\right)$$

For weak to strong inversion, the empirical model yields:

$$CsrTR \equiv \frac{I_D}{g_m^{1/2}} = \sqrt{n v_{th} I_o W\left(K\ e^{\frac{\beta V_G}{n}}\right)\left[1 + W\left(K\ e^{\frac{\beta V_G}{n}}\right)\right]}$$

$$V_G = n v_{th}\left[\ln\left(-1 + \sqrt{1 + \frac{4\,CsrTR^2}{n v_{th} I_o}}\right) + \frac{1}{2}\sqrt{1 + \frac{4\,CsrTR^2}{n v_{th} I_o}} - 1/2 - \ln(2K)\right]$$

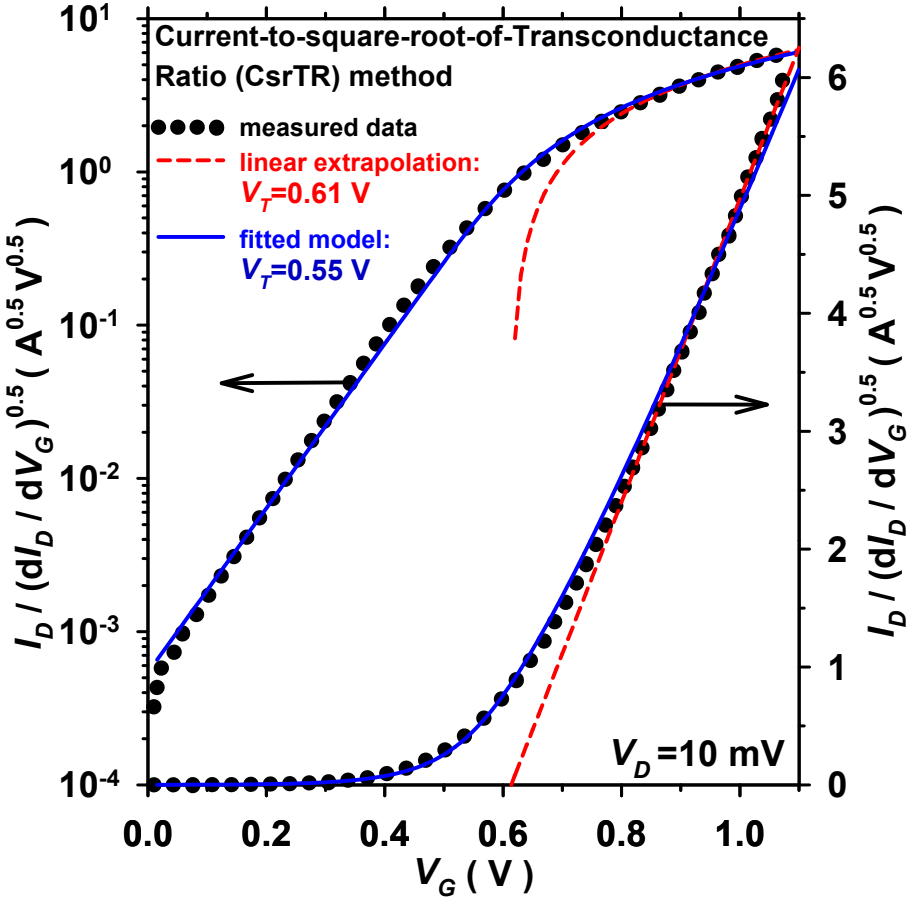
[JA88] Jain S. Measurement of threshold voltage and channel length of submicron MOSFETs." IEE Proc. Cir. Dev. and Sys. 1988; 135: 162.

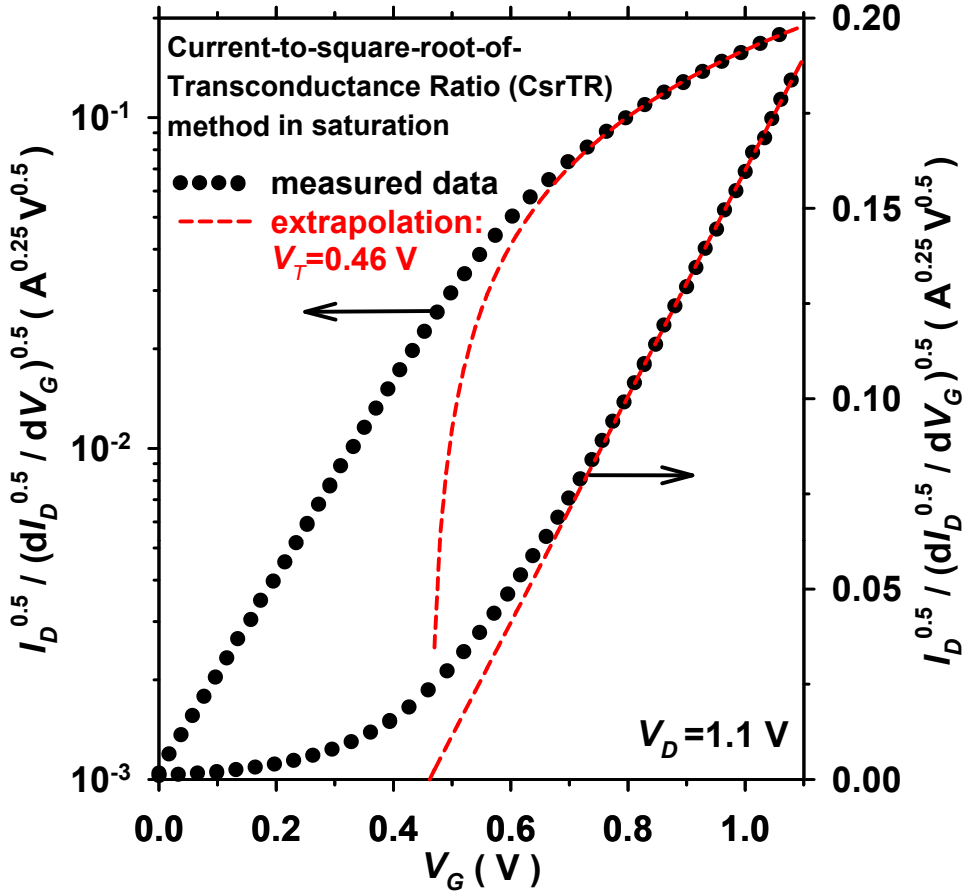
[GH88] Ghibaudo G. New method for the extraction of MOSFET parameters. Electronics Letters 1988; 24: 543–545.

[FI95] Fikry W, Ghibaudo G, Haddara H, Cristoloveanu S, Dutoit M. Method for extracting deep submicrometer MOSFET parameters. Electron. Lett. 1995; 31: 762-764.

[SU10] Subramanian, N., Ghibaudo, G., Mouis, M., "Parameter extraction of nano-scale MOSFETs using modified Y function method", Proceedings of the European Solid State Device Research Conference, ESSDERC 2010 , art. no. 5618348 , pp. 309-312, 2010.

[JO11] Jomaah, J., Fadlallah, M., Ghibaudo, G., "DC characterization of different advanced MOSFET architectures", Advanced Materials Research 324 , pp. 407-410, 2011.





$$CsrTR \equiv \frac{I_D}{\sqrt{dI_D/dV_G}}$$

$$CsrTR_{sat} \equiv \frac{\sqrt{I_D}}{\sqrt{d\sqrt{I_D}/dV_G}}$$

Tsormpatzoglou et al [TS12] recently proposed an improvement of the current-to-square-root-Transconductance Ratio (CsrTR) method.

A simplified variation of this method will now be described.

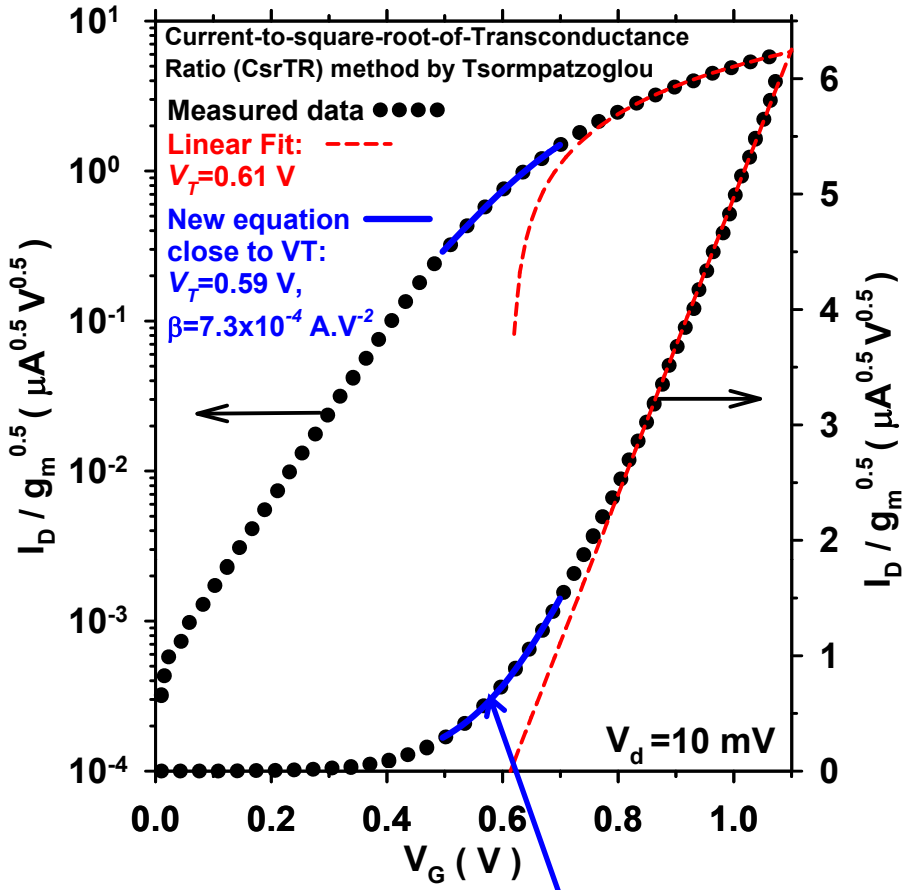
The following equation is valid for weak to strong inversion:

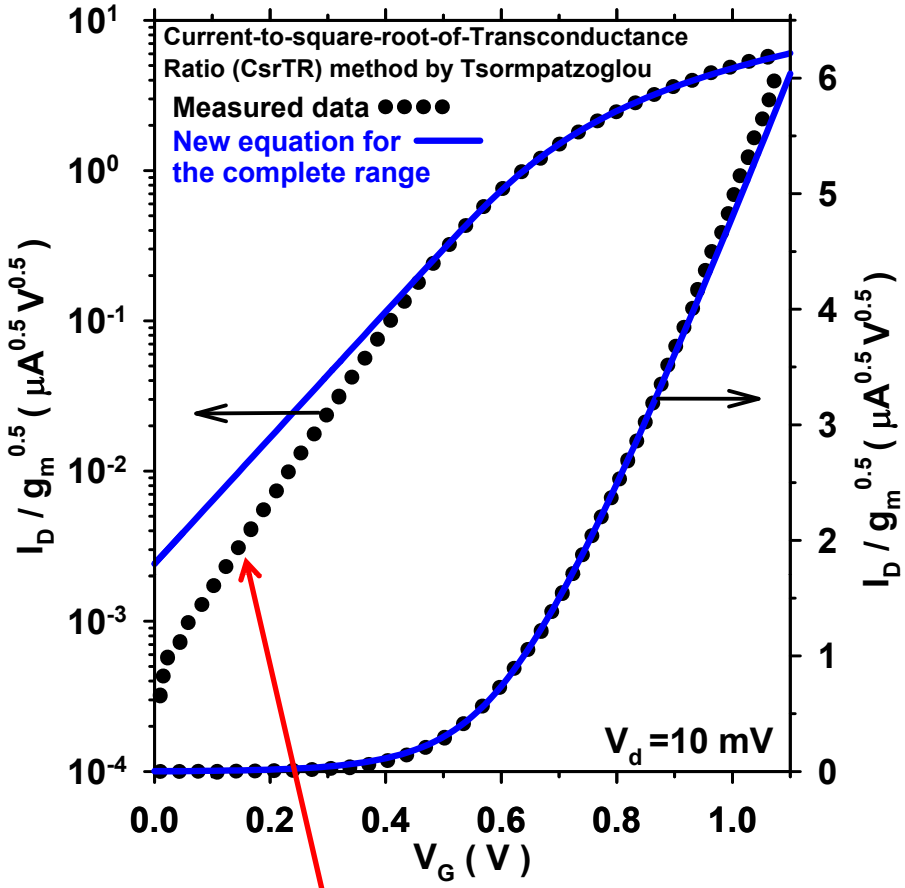
$$V_g = V_T + v_{th}\, ln\left(\frac{e^{\left(\frac{4\,CsrTR^2}{B^2+\sqrt{B^4+4B^2CsrTR^2}}\right)}\left(B^2 - \sqrt{B^4+4B^2CsrTR^2}\right)^2}{4B^4} \right)$$

where $B \equiv 2v_{th}\sqrt{\beta V_d}$

In order to extract V_T and β, and avoid second order effects, the previous equation is fitted for values close to V_T.

[TS12] Tsormpatzoglou, A., Papathanasiou, K., Fasarakis, N., Tassis, D.H., Ghibaudo, G., Dimitriadis, C.A., "A Lambert-function charge-based methodology for extracting electrical parameters of nanoscale FinFETs", IEEE Transactions on Electron Devices 59 (12) , art. no. 6343230 , pp. 3299-3305, 2012.





The range of V_G, for extracting V_T and β, is estimated by the linear fit method.

The model presents serious errors for weak inversion.

Comparison of the equation proposed by Tsormpatzoglou and our empirical model

The equation proposed by Tsormpatzoglou is simplified to:

$$V_G = V_T - 2ln(2)v_{th} + 2v_{th}\, ln\left(\sqrt{1+4\left(\frac{CsrTR}{B}\right)^2} - 1\right) + \frac{4v_{th}\left(\frac{CsrTR}{B}\right)^2}{\left(\sqrt{1+4\left(\frac{CsrTR}{B}\right)^2} + 1\right)}$$

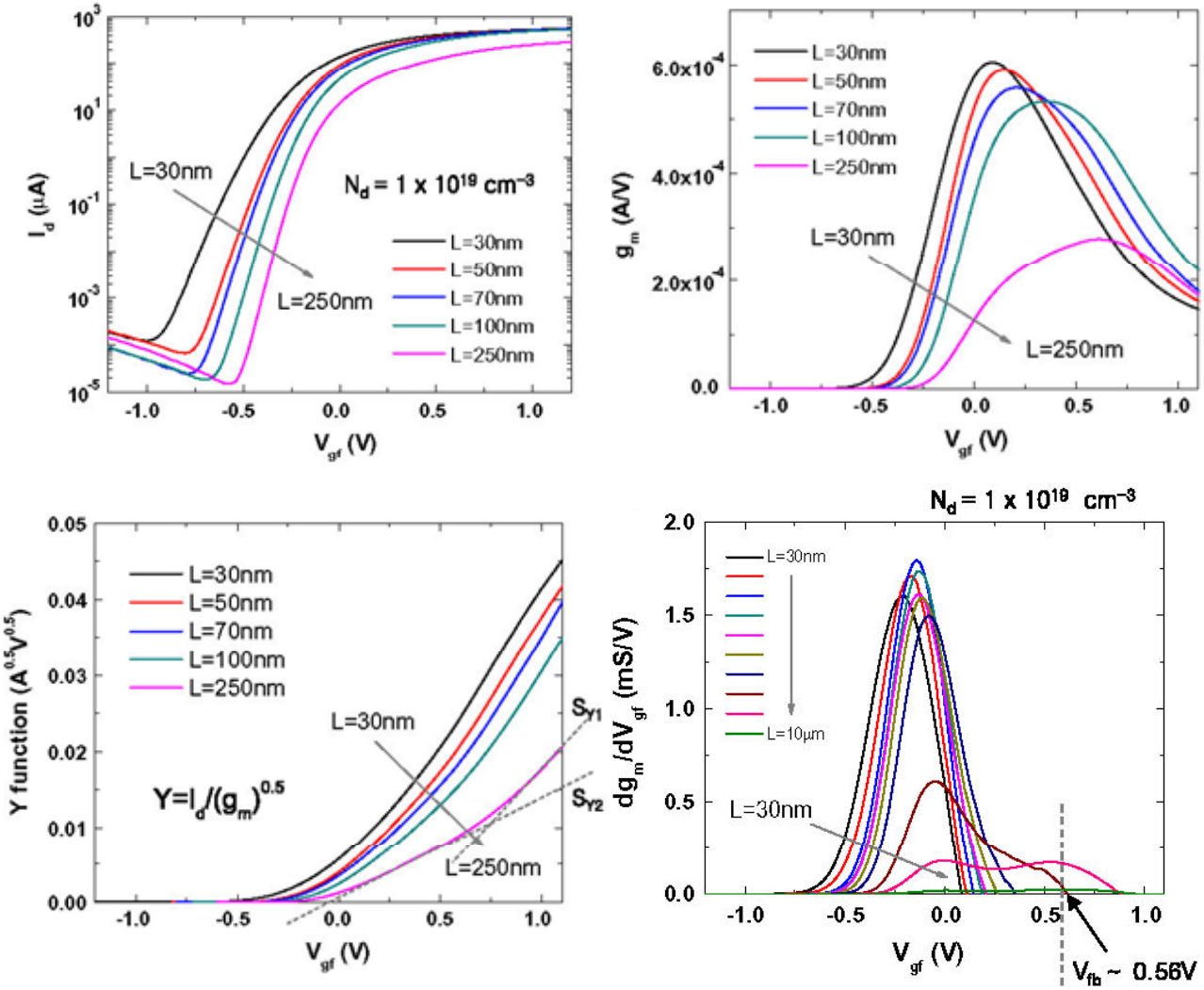
Our empirical model is:

$$V_G = V_T - n v_{th}\ln(2K) + n v_{th}\ln\left(-1+\sqrt{1+\frac{4CsrTR^2}{n v_{th} I_o}}\right) + \frac{n v_{th}}{2}\left(\sqrt{1+\frac{4CsrTR^2}{n v_{th} I_o}} - 1\right)$$

The models are different although they present some similarities.

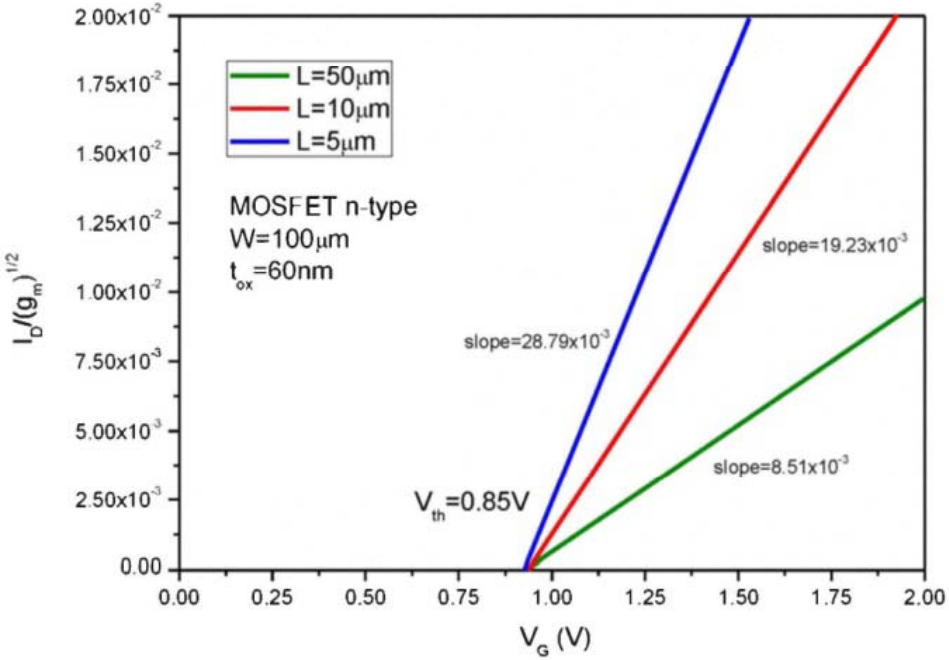
Jeon et al recently applied [JE13] the current-to-square-root-Transconductance Ratio (CsrTR) method to junctionless transistors

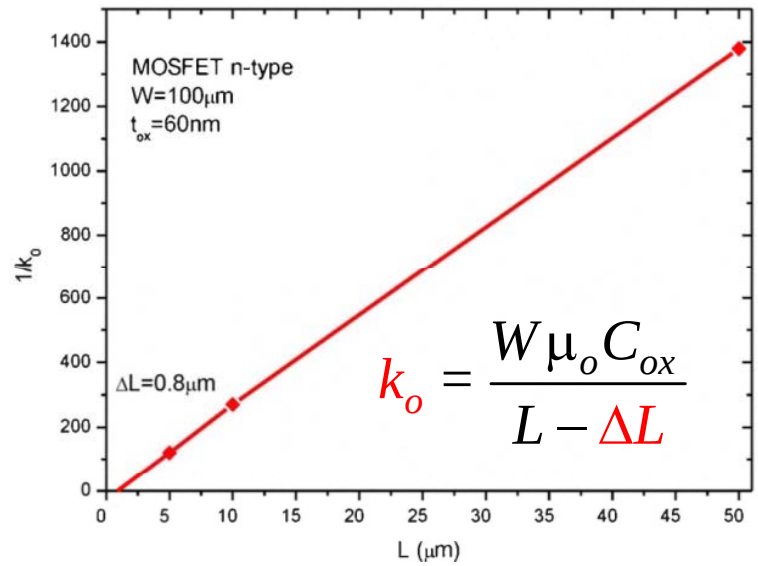
The CsrTR method could yields to two slopes.
The SD method could also yields to two V_T.
For $V_G << V_{FB}$ the device is in full depletion.
When $V_G = V_{FB}$, the device becomes neutral.
For $V_G >> V_{FB}$, the device is in accumulation.
Therefore, there are two successive conduction regimes separated by V_{FB} : volume and accumulation conduction.



[JE13] D.-Y. Jeon, S.J. Park, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim, G. Ghibaudo, "Revisited parameter extraction methodology for electrical characterization of junctionless transistors·, Solid-State Electronics, In Press, Available online 19 March 2013.

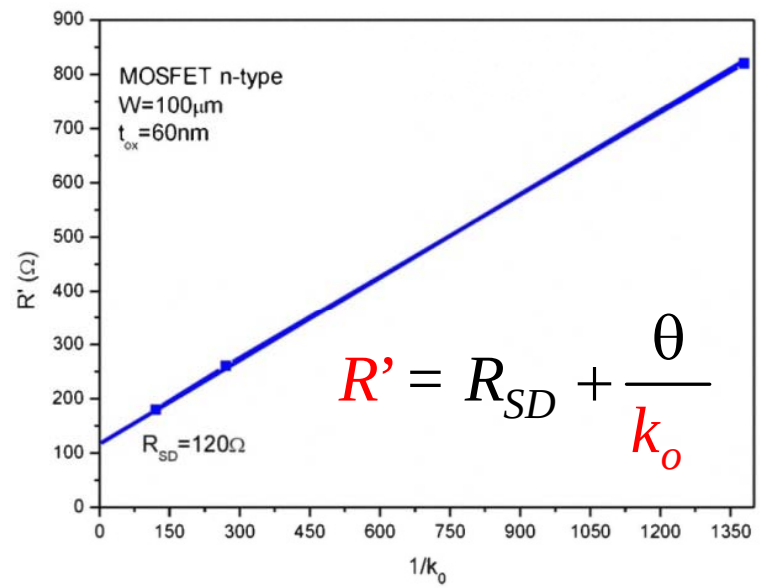
Ortega and coworkers from INAOE [OR10] also used the current-to-square-root-Transconductance Ratio (CsrTR) method.





$$k_o = \frac{W \mu_o C_{ox}}{L - \Delta L}$$

$$CsrTR = \sqrt{k_o V_D}\,(V_G - V_T)$$



$$R' = R_{SD} + \frac{\theta}{k_o}$$

V_T, the effective channel, the series resistance and the mobility degradation are extracted.

[OR10] Ortega, R., Molina, J., Torres, A., Landa, M., Alarcón, P., Escobar, M., "Extraction of gate oxide quality and its correlation to the electrical parameters of MOS devices", IEEE EDSSC, art. no. 5713676, 2010.

Emrani et al [EM93] generalized the CsrTR method to account for other mobility models at low temperature.

Assuming a mobility model such as

$$I_D = K \frac{(V_G - V_T)^{n-1}}{\left(1+\theta^{n-1}(V_G - V_T)^{n-1}\right)}$$

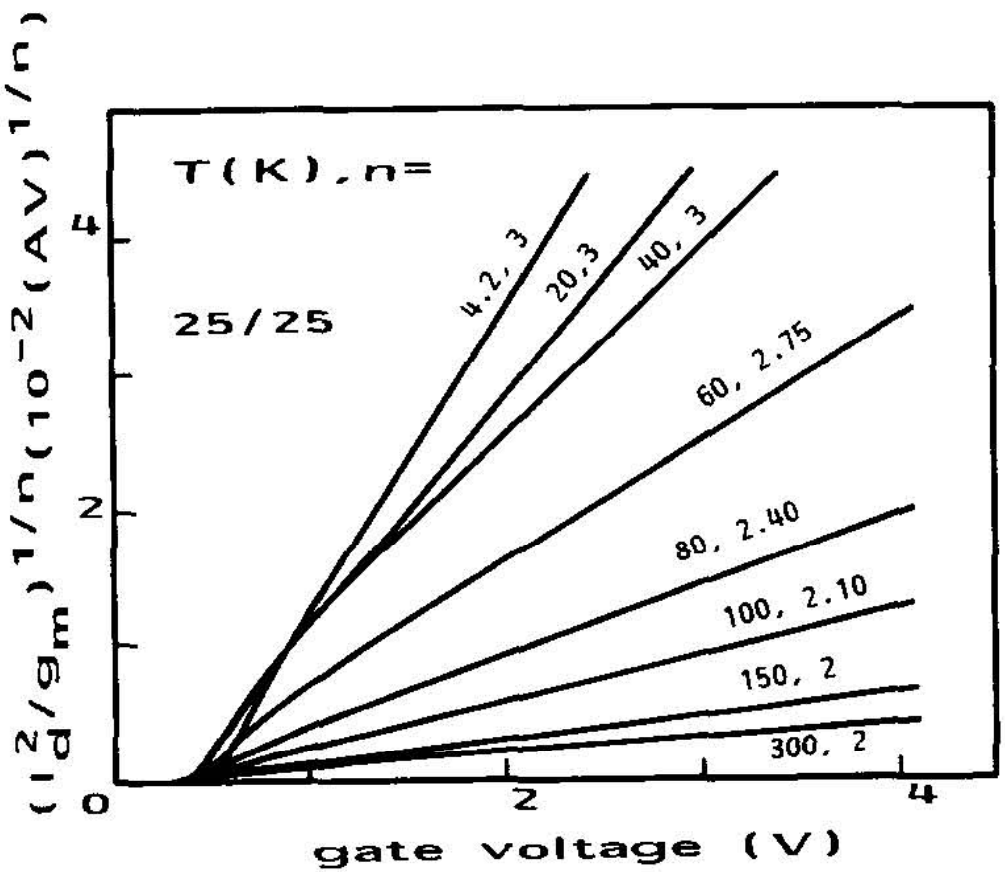
It can be proved:

$$CsrTR \propto (V_G - V_T)^{2/n}$$

For n=3:

$$I_D = K \frac{(V_G - V_T)^{2}}{\left(1+\theta^{2}(V_G - V_T)^{2}\right)}$$

$$CsrTR \propto (V_G - V_T)^{2/3}$$



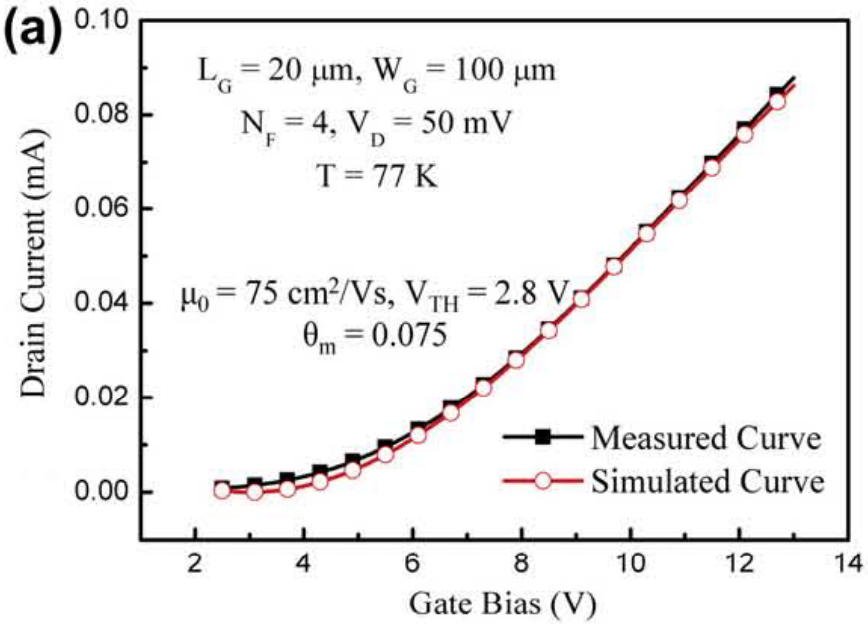
[EM93] Emrani, A., Balestra, F., Ghibaudo, G., "Generalized mobility law for drain current modeling in Si MOS transistors from liquid helium to room temperatures", 1993, IEEE Transactions on Electron Devices 40 (3) , pp. 564-569.

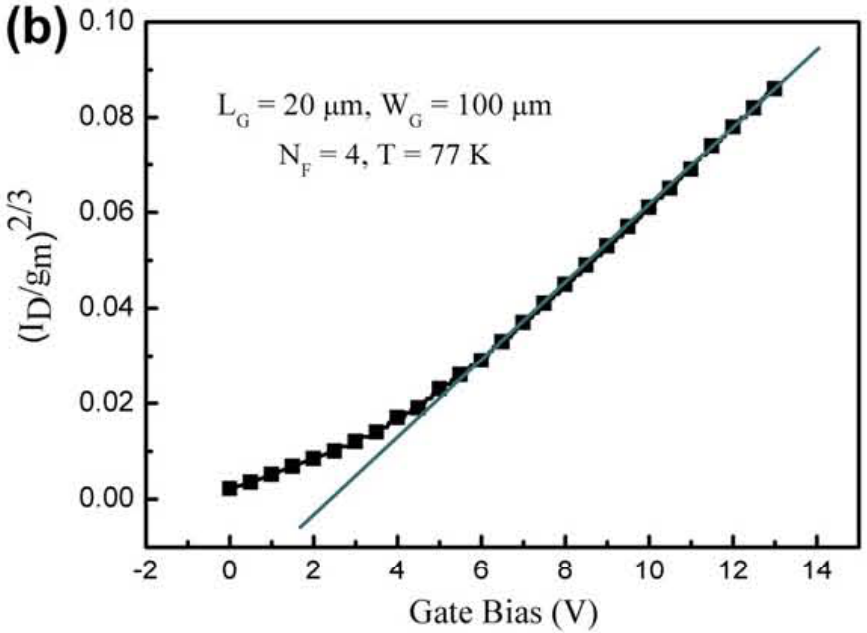
The previous generalization has been recently used [CH12;13] for nanocrystalline ZnO thin film transistors

They used n=3:

$$I_D = K \frac{(V_G - V_T)^2}{\left(1 + \theta^2 (V_G - V_T)^2\right)}$$

$$CsrTR \propto (V_G - V_T)^{2/3}$$





[CH13] Chang, S.-J., Cheralathan, M., Bawedin, M., Iniguez, B., Bayraktaroglu, B., Lee, J.-H., Lee, J.-H., Cristoloveanu, S., "Mobility behavior and models for fully depleted nanocrystalline ZnO thin film transistors", 2013, Solid-State Electronics, Article in Press.

[CH12] Cheralathan, M., Chang, S.J., Bawedin, M., Bayraktaroglu, B., Lee, J.H., Iniguez, B., Cristoloveanu, S., "Mobility models for ZnO TFTs", ICCDCS 2012 , art. no. 6188880.

2.7. Transition method

This method [GA00] was inspired on the integral difference function *D*, which was defined for a two-terminal device as [GA95,96]:

$$D(V,I) \equiv \int_0^I V dI - \int_0^V I dV = VI - 2\int_0^V I dV$$

This function has the property of eliminating the effect of any resistance connected in series with the device.

The transition method proposes to use the function G_1:

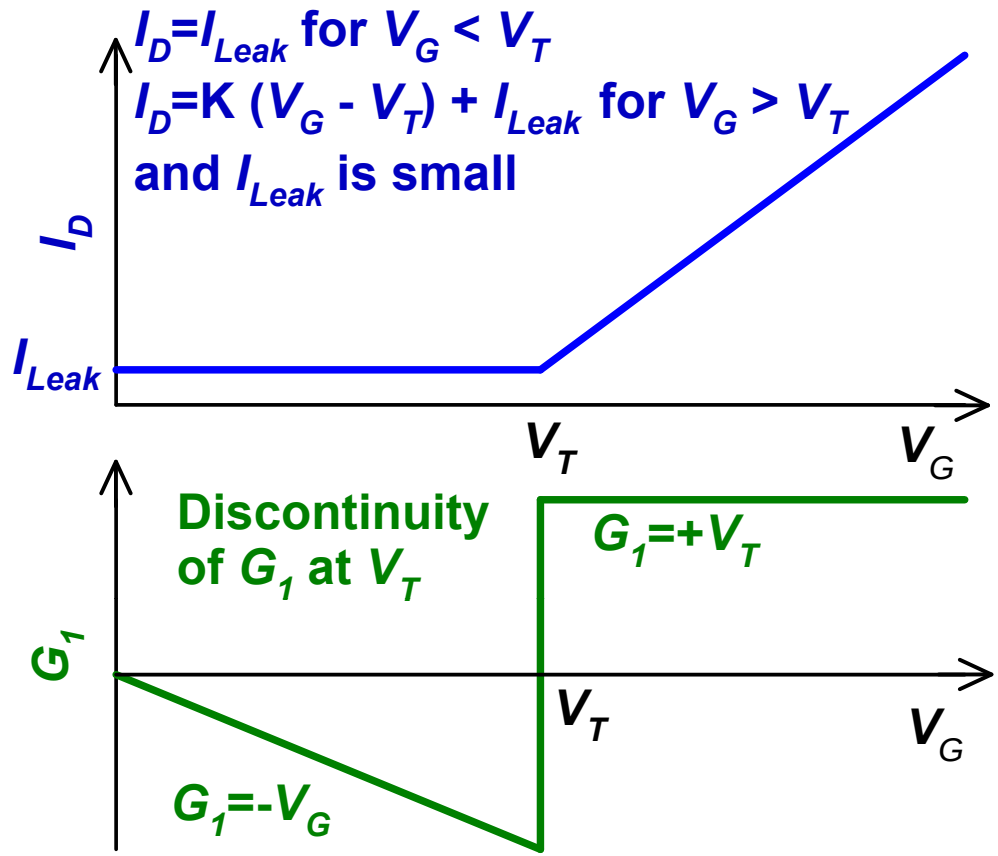
$$G_1(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D} = \left(V_G - V_{Gi}\right) - 2\,\frac{\int_{V_{Gi}}^{V_G} I_D\, dV_G}{I_D}$$

[GA95] García Sánchez FJ, Ortiz-Conde A, De Mercato G, Liou JJ, Recht L. Eliminating parasitic resistances in parameter extraction of semiconductor device models. Proc. of First IEEE Int. Caracas Conf. on Dev. Cir. and Sys. 1995; Caracas, Venezuela, 298.

[GA96] García Sánchez FJ, Ortiz-Conde A, Liou JJ. A parasitic series resistance-independent method for device-model parameter extraction, IEE Proc. Cir. Dev. and Sys. 1996; 143, 68.

[GA00] García Sánchez FJ, Ortiz-Conde A, Mercato GD, Salcedo JA, Liou JJ, Yue Y. New simple procedure to determine the threshold voltage of MOSFETs. Solid-St. Electron, 2000; 44; 673-675.

The origin of the **transition method** can be understood by analyzing the ideal case of a MOSFET: $I_D = I_{Leak}$ for $V_G < V_T$ and $I_D \propto V_G$ for $V_G > V_T$.



Using these assumptions, we observe that:

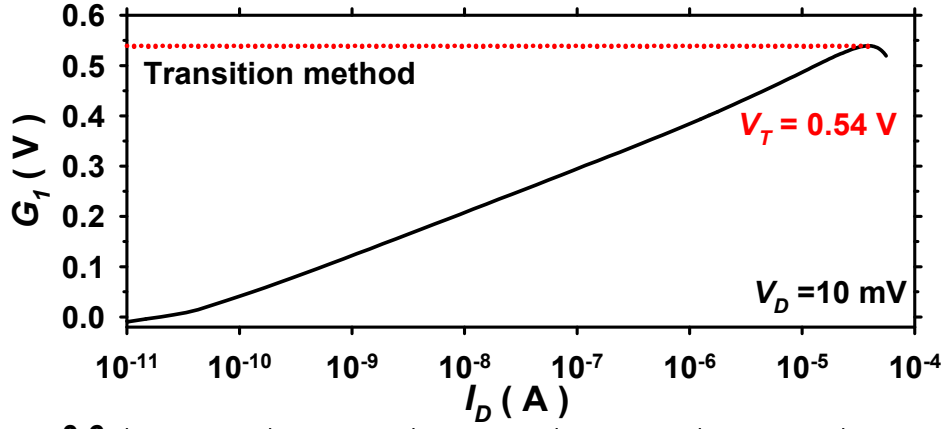
(a) G_1 has a discontinuity at V_T;

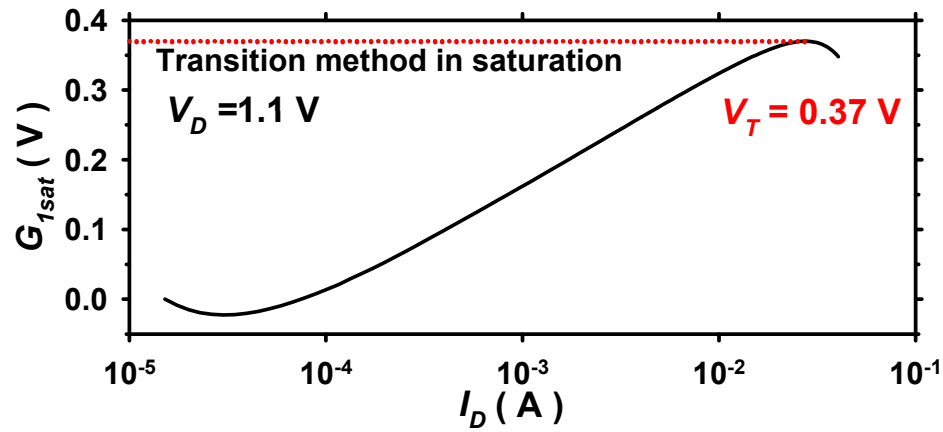
(b) $G_1 = -V_G$ for $V_G < V_T$; and

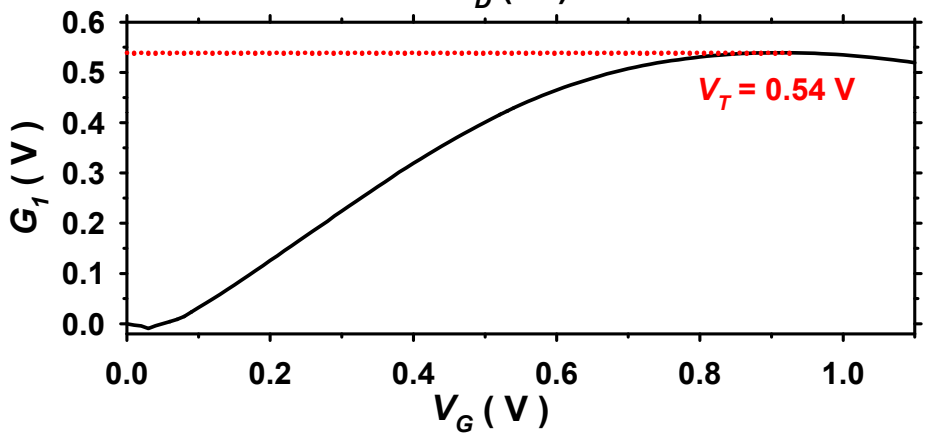
(c) $G_1 = +V_T$ for $V_G > V_T$.

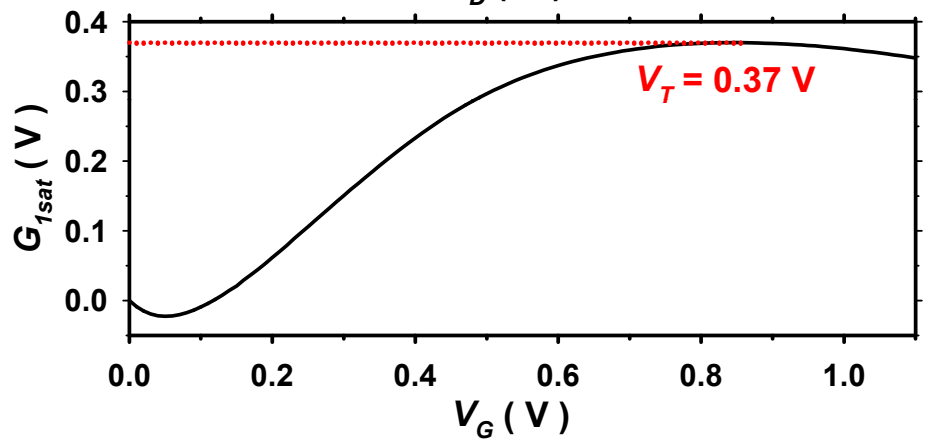
For a real device function G_1 will have a maximum due to the mobility degradation and its value will be close to V_T.

$$G_1 = V_G - 2\,\frac{\int_0^{V_G} I_D\, dV_G}{I_D}$$









$$G_1(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D} = (V_G - V_{Gi}) - 2\,\frac{\int_{V_{Gi}}^{V_G} I_D\, dV_G}{I_D}$$

$$G_{1sat}(V_G, I_D) = (V_G - V_{Gi}) - 2\,\frac{\int_{V_{Gi}}^{V_G} \sqrt{I_D}\, dV_G}{\sqrt{I_D}}$$

2.8. Normalized Mutual Integral Difference (NMID) Method

This method [HE02] is inspired in normalizing the function *D*:

$$D_{normal}(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D V_G} = 1 - 2\,\frac{\int_0^{V_G} I_D\, dV_G}{I_D V_G}$$

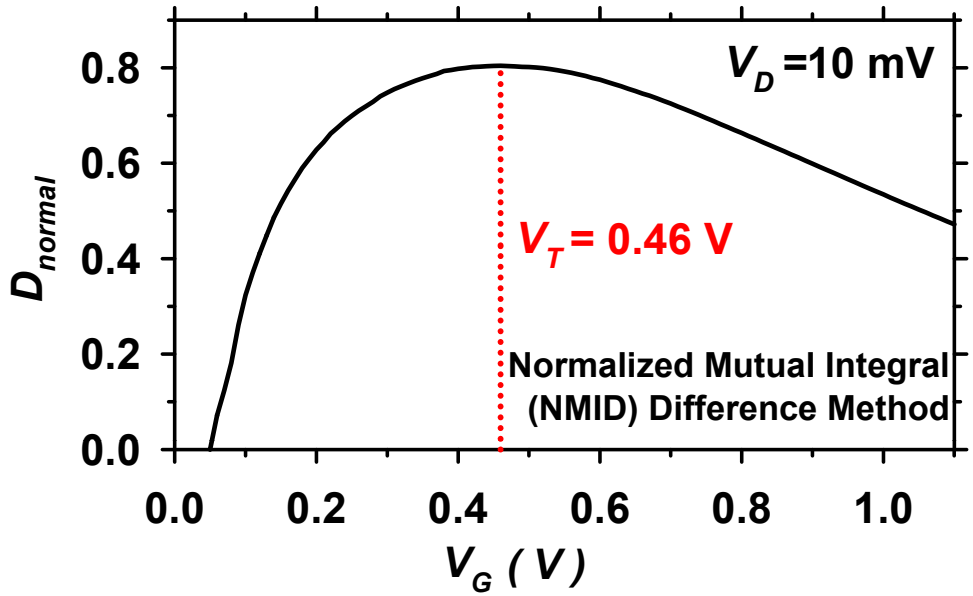
Accordingly, a plot of D_{normal} versus V_G will have a maximum at the value of V_T.

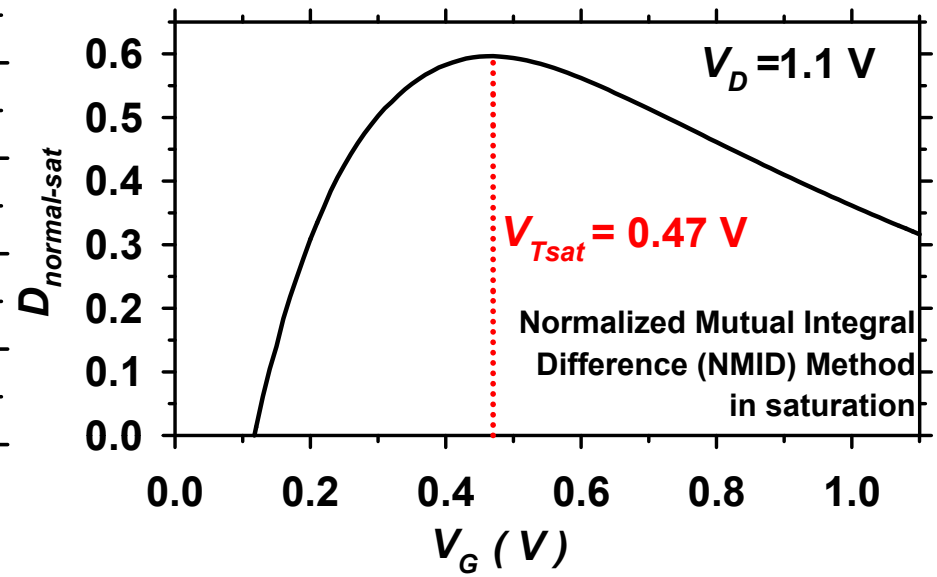
Notice that the location of a maximum is independent of the constant and thus, the term "-1" can be removed.

A disadvantage of this method is that the maximum is located in a broad region.

In the next section we will present an improvement of the present method.

[HE02] He, J., Xi, X., Chan, M., Cao, K., Hu, C., Li, Y., Zhang, X., Huang R., and, Wang, Y., "Normalized mutual integral difference method to extract threshold voltage of MOSFETs", IEEE Electron Device Letters 23 (7) , pp. 428-430, 2002.





$$D_{normal}(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D V_G} = 1 - 2\,\frac{\int_0^{V_G} I_D\, dV_G}{I_D V_G}$$

$$D_{normal-sat}(V_G, \sqrt{I_D}) \equiv 1 - 2\,\frac{\int_0^{V_G} \sqrt{I_D}\, dV_G}{\sqrt{I_D}\, V_G}$$

2.9. Normalized Reciprocal H (NRH) function method

By removing the -1 term and the factor 2 from the previous method and considering that the current is not zero at V_G =0, we can obtain a normalized version of our previous *H* function which was originally proposed in 2001 [OR01] for extracting the threshold voltage of amorphous thin film MOSFETs, and it was revised in 2010 [OR10] to evaluate the sub-threshold slope of MOSFETs:

$$H_{normal}\left(V_G\right) = \frac{\int_0^{V_G} I_D(V_G)\, dV_G}{V_G\left[I_D - I_D\left(V_G = 0\right)\right]}$$

[OR01] Ortiz-Conde A, Cerdeira A, Estrada M, García Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. Solid-State Electronics 2001; 45: 663-667.

[OR10] Ortiz-Conde, A., García-Sánchez, F.J., Liou, J.J., Ho, C.-S., "Integration-based approach to evaluate the sub-threshold slope of MOSFETs", Microelectronics Reliability 50 (2) , pp. 312-315, 2010.

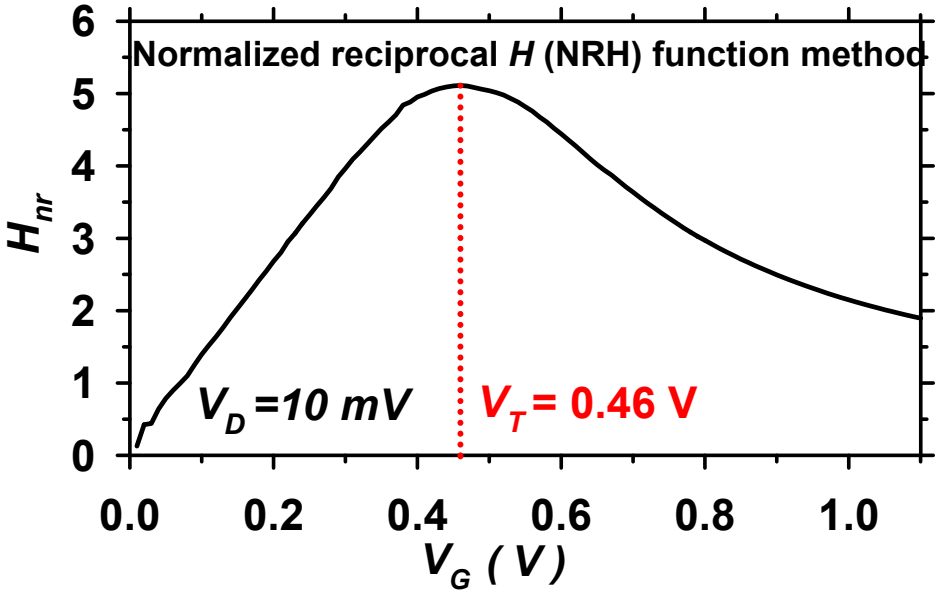
In order to obtain results with maximum or minimum in narrow regions, we propose to use the reciprocal of the previous function:

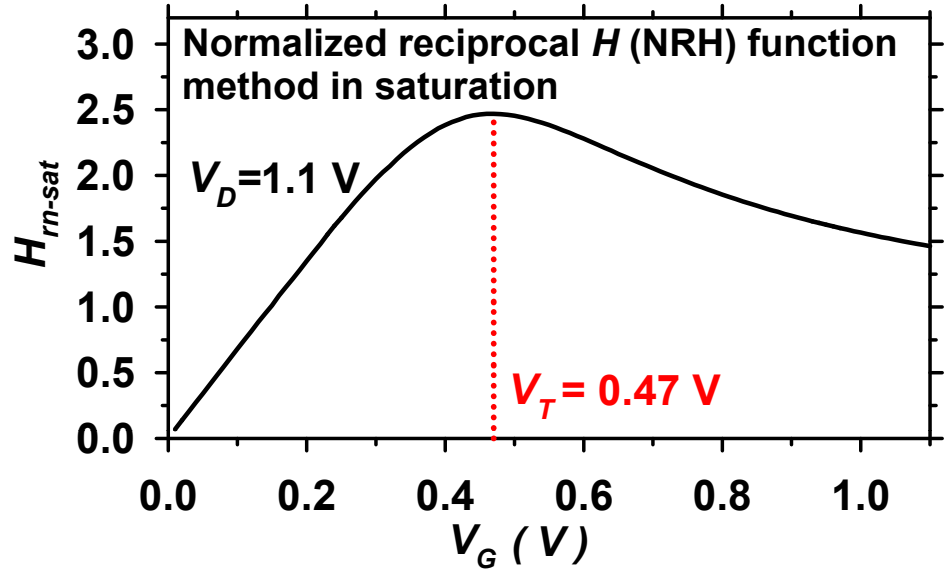
$$H_{nr}\left(V_G\right) = \frac{V_G\left[I_D - I_D\left(V_G = 0\right)\right]}{2\int_0^{V_G} I_D(V_G)\, dV_G}$$

A factor of 2 was included in order to obtain the following simple graphical interpretation:

1. The numerator divided by 2 is the area of a triangle with a width of V_G and a height of ($I_D - I_D(V_G = 0)$).

2. Then, H_{nr} is the ratio of the area of this triangle divided by the area under the plot (the integration).





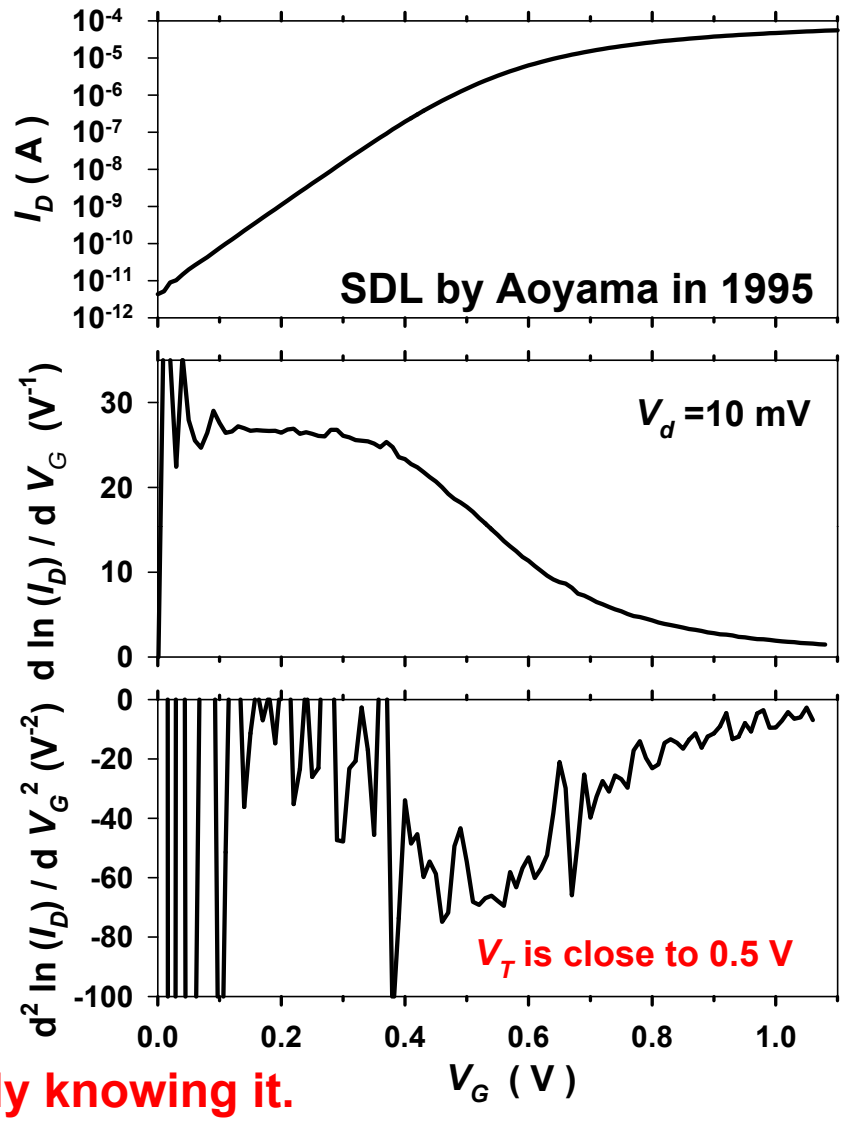
$$H_{nr}\left(V_G\right)=\frac{V_G\left[I_D-I_D\left(V_G=0\right)\right]}{2\int_0^{V_G} I_D(V_G)\,dV_G}$$

$$H_{nr-sat}\left(V_G\right)=\frac{V_G\left[\sqrt{I_D}-\sqrt{I_D\left(V_G=0\right)}\right]}{2\int_0^{V_G}\sqrt{I_D}\,dV_G}$$

2.10. Transconductance-to-Current-Ratio (TCR) methods

The function g_m/I_D has been used for device characterization for more than 3 decades [TS82]:

$$TCR = \frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{d\ \ln\left(I_D\right)}{dV_G}$$



2.10.1 SDL by Aoyama in 1995 [AO95]

The TCR methods can be related to the pioneering publication by Aoyama in 1995 [AO95], who proposed that V_T be determined as the gate voltage at which the Second Derivative of the Logarithm (SDL) of the drain current takes on a minimum value:

$$V_T \equiv V_G \ \ at \ \left.\frac{d^2 \ln\left(I_D\right)}{dV_G^2}\right|_{\min}$$

Measurement noise is significant.

Aoyama was using TCR without probably knowing it.

[TS82] Tsividis Y. Moderate inversion in MOS devices. Solid-State Electron, 25, pp. 1099–104, 1982.

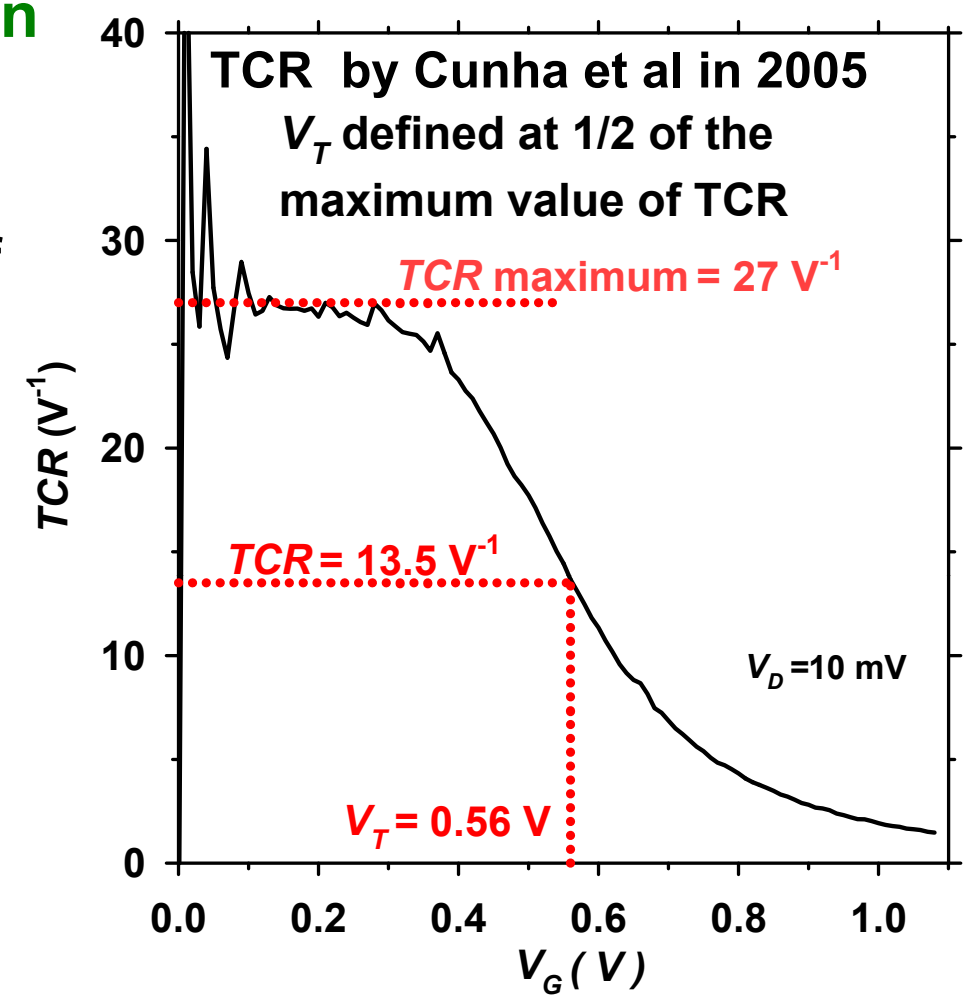
[AO95] Aoyama K. A method for extracting the threshold voltage of MOSFET based on current components . Simulation of Semiconductor Devices and Processes 1995; 6: 118-121.

2.10.2 TCR by Cunha et al in 2005 [CU05;GA07]

They proposed [CU05;GA07] that V_T be determined as the value of V_G at which TCR is equal to half of its maximum value.

$$V_T \equiv V_G \quad at \quad \frac{TCR_{\max}}{2}$$

This definition has been related [CU11,SI12] to the condition that diffusion and drift current be equal.



[CU05] A. I. A. Cunha, M. C. Schneider, C. Galup-Montoro, C. D. C. Caetano, and M. B. Machado, "Unambiguous Extraction of Threshold Voltage Based on the Transconductance-to-Current Ratio", WCM Nanotech, pp. 139-141, 2005.
[GA07] C. Galup-Montoro and M. C. Schneider, "Mosfet Modeling For Circuit Analysis And Design", World Scientific, 2007.
[CU11] Cunha, A.I.A., Pavanello, M.A., Trevisoli, R.D., Galup-Montoro, C., Schneider, M.C., "Direct determination of threshold condition in DG-MOSFETs from the g m/ID curve", Solid-State Electronics 56 (1) , pp. 89-94, 2011.
[SI12] Siebel, O.F., Schneider, M.C., Galup-Montoro, C., "MOSFET threshold voltage: Definition, extraction, and some applications", Microelectronics Journal 43 (5) , pp. 329-336, 2012.

Doria et al [DO13] recently applied the TCR method to junctionless transistors

The previous definition of V_T (V_G at which TCR is equal to half of its maximum value) was recently used [DO13] for junctionless nanowire transistors.

Numerical simulations [DO13] show that this definition coincides with the condition that diffusion and drift current be equal.

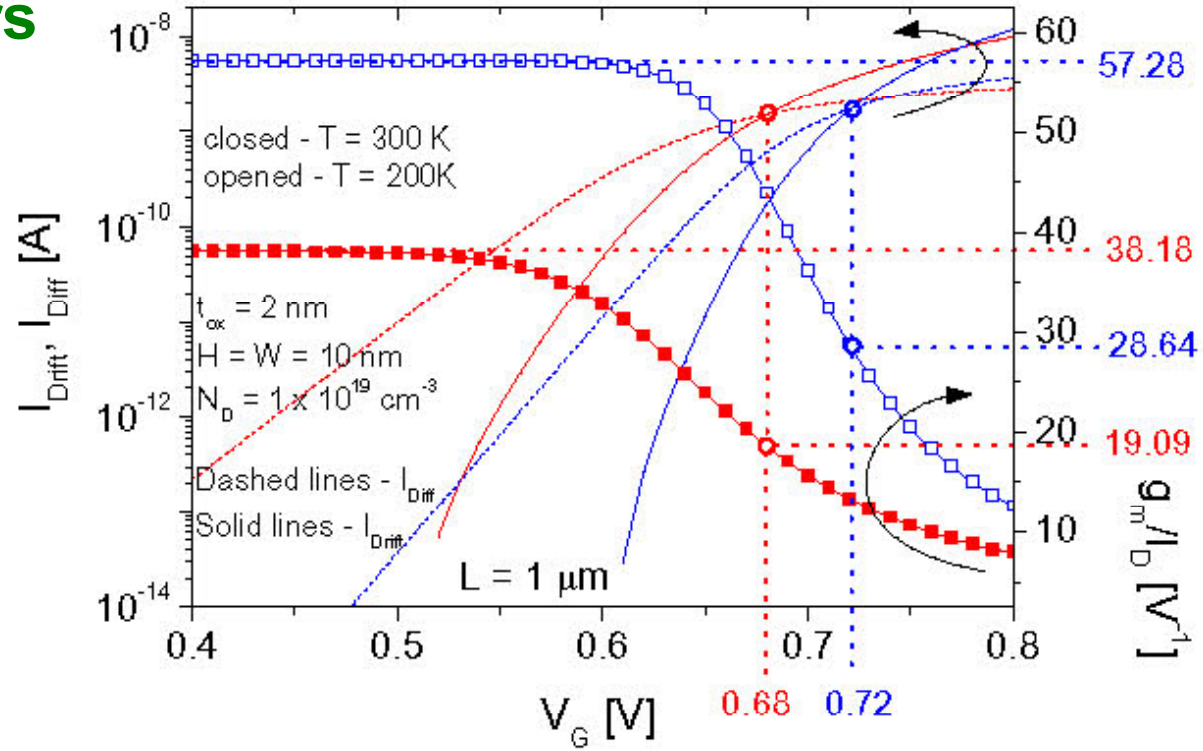


Fig. 3 in [DO13] "Drift and diffusion components of the current (left axis) and the transconductance to the current ratio (right axis) as a function of the gate voltage for two temperatures".

[DO13] Renan Doria Trevisoli, Rodrigo Trevisoli Doria, Michelly de Souza, Marcelo Antonio Pavanello, "A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors", Solid-State Electronics, In Press, Available online 19 March 2013.

2.10.3 TCR by Flandre and his group in 2010 [FL10]

They proposed [FL10] that V_T be defined at the location of the maximum slope of TCR. Using:

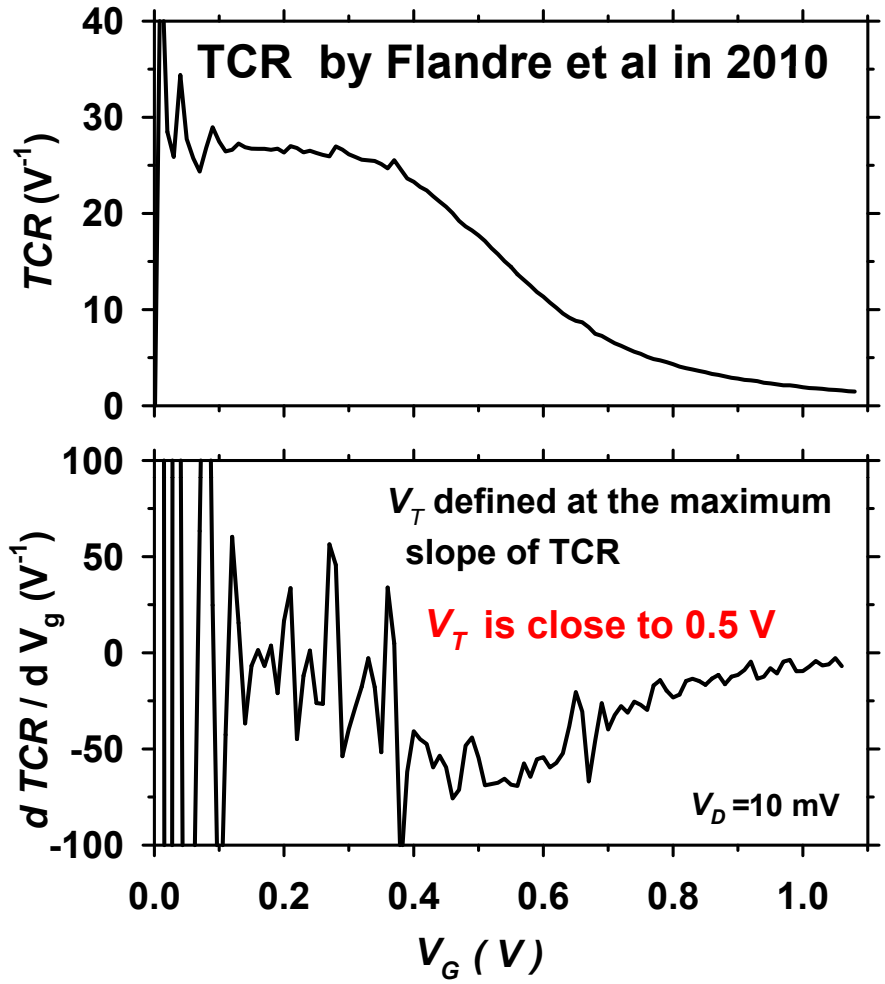
$$\frac{d^2 \ln(I_D)}{dV_G^2} = \frac{d\ TCR}{dV_G}$$

$$\Rightarrow V_T \equiv V_G \ at \left| \frac{d\,TCR}{dV_G} \right|_{\max}$$

$$\equiv V_G \ at \left. \frac{d\,TCR}{dV_G} \right|_{\min} = V_G \ at \left. \frac{d^2 \ln(I_D)}{dV_G^2} \right|_{\min}$$

Therefore, this definition is mathematically equivalent to SDL. It has been related to the threshold voltage obtained from C-V.

Measurement noise is significant.



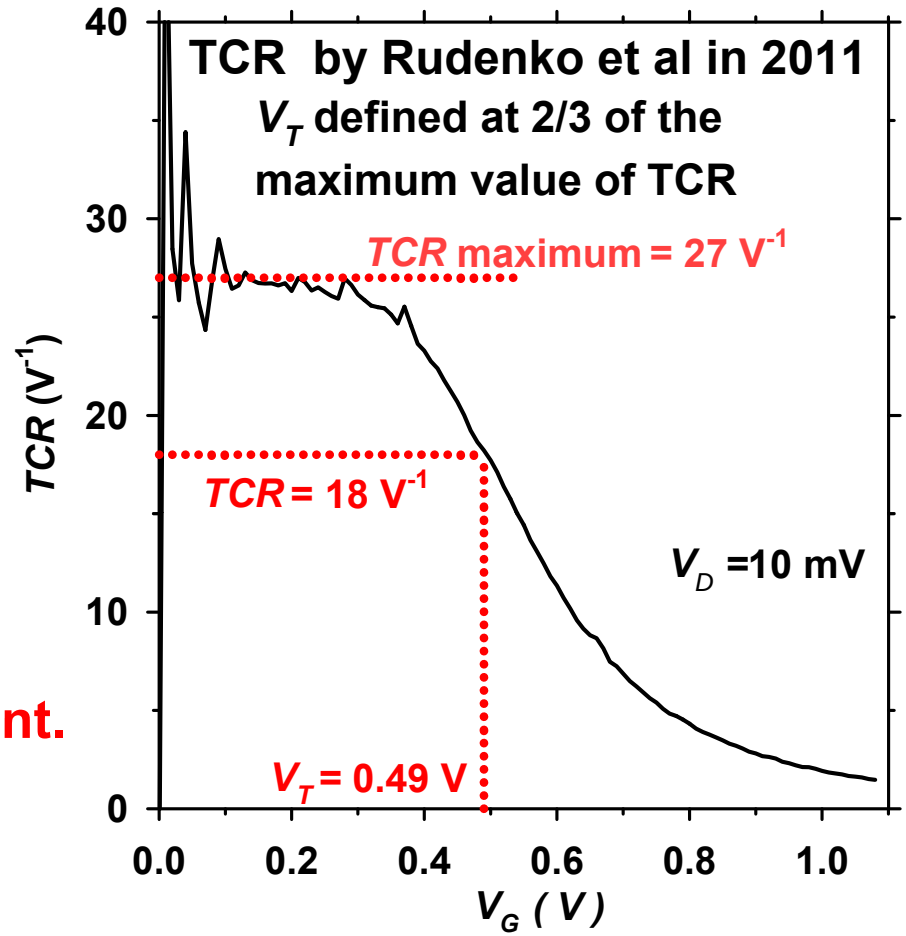
[FL10] Flandre, D., Kilchytska, V., Rudenko, T., "Gm/Id method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold", IEEE Electron Device Letters 31 (9) , art. no. 5545349 , pp. 930-932, 2010.

2.10.4 TCR by Rudenko et al in 2011 [RU11a,b]

In order to reduce the noise effects due to the derivative, they proposed [RU11a,b] to define the threshold voltage as the gate bias at which TCR is 2/3 of its maximum value.

$$V_T \equiv V_G \quad at \quad \frac{2\,TCR_{\max}}{3}$$

Measurement noise is not significant.



[RU11a] Rudenko, T., Kilchytska, V., Arshad, M.K.M., Raskin, J.-P., Nazarov, A., Flandre, D. "On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part I-Effect of gate-voltage-dependent mobility", IEEE Transactions on Electron Devices 58 (12) , art. no. 6046124 , pp. 4172-4179, 2011.
[RU11b] Rudenko, T., Kilchytska, V., Md Arshad, M.K., Raskin, J.-P., Nazarov, A., Flandre, D., "On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part II-Effect of drain voltage", IEEE Transactions on Electron Devices 58 (12) , art. no. 6046226 , pp. 4180-4188, 2011.

2.11. Reciprocal H (RH) methods

TCR **(=g_m/I_D) is equivalent to the inverse of the sub-threshold slope factor:**

$$S = \frac{\ln(10)}{\dfrac{d\,\ln(I_D)}{d\,V_G}} = \frac{I_D}{g_m}\ln(10)$$

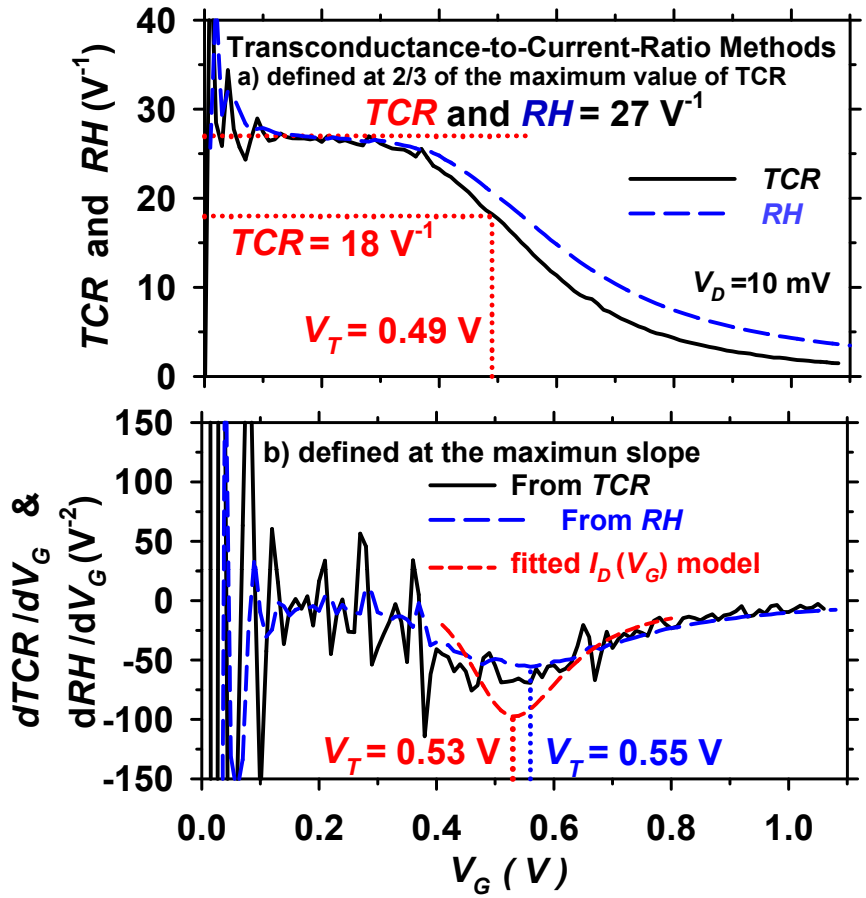
Considering that *TCR* significantly increases measurement noise, especially in weak inversion, an equivalent function for low gate bias, based on integrations was proposed in 2010 [OR10] :

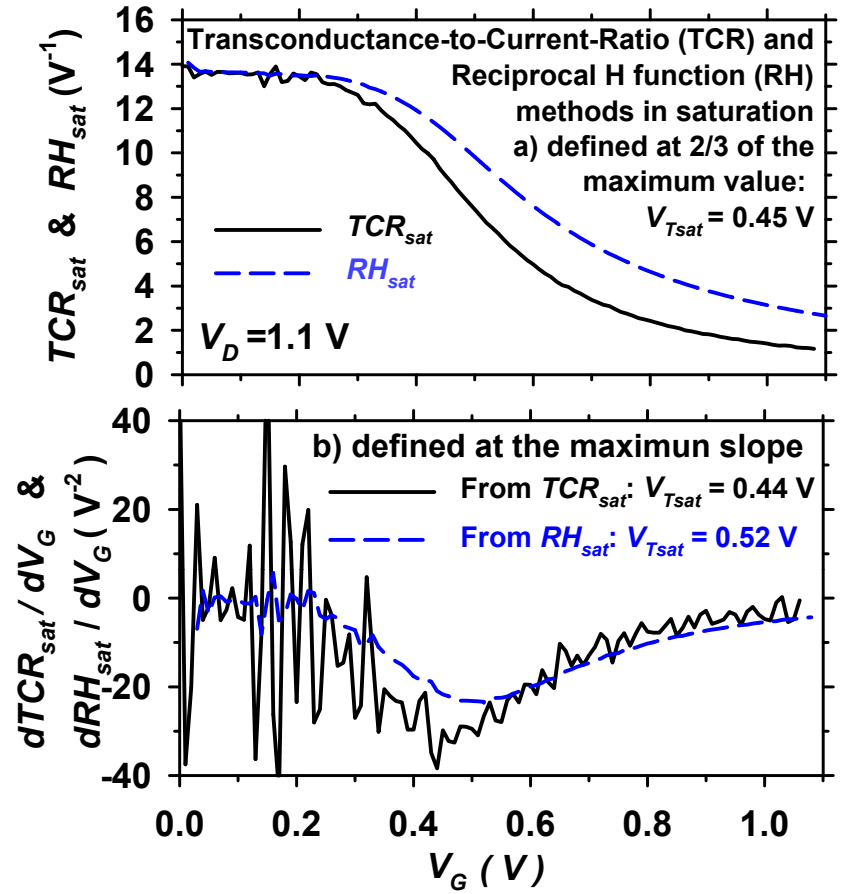
$$H_r(V_G) = \frac{\left[I_D - I_D(V_G = 0)\right]}{\int_0^{V_G} I_D(V_G)\,dV_G}$$

The RH method [OR13] proposes that V_T be defined by the maximum slope of function H_r.

[OR10] Ortiz-Conde, A., García-Sánchez, F.J., Liou, J.J., Ho, C.-S., "Integration-based approach to evaluate the sub-threshold slope of MOSFETs", Microelectronics Reliability 50 (2) , pp. 312-315, 2010.

[OR13] A. Ortiz-Conde, F.J. García-Sánchez, J. Muci, A. Terán Barrios, J.J. Liou,, C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods", Microelectronics Reliability 53 (1) , pp. 90-104, 2013.





$$TCR = \frac{d \ \ln\left(I_D\right)}{d V_G}$$

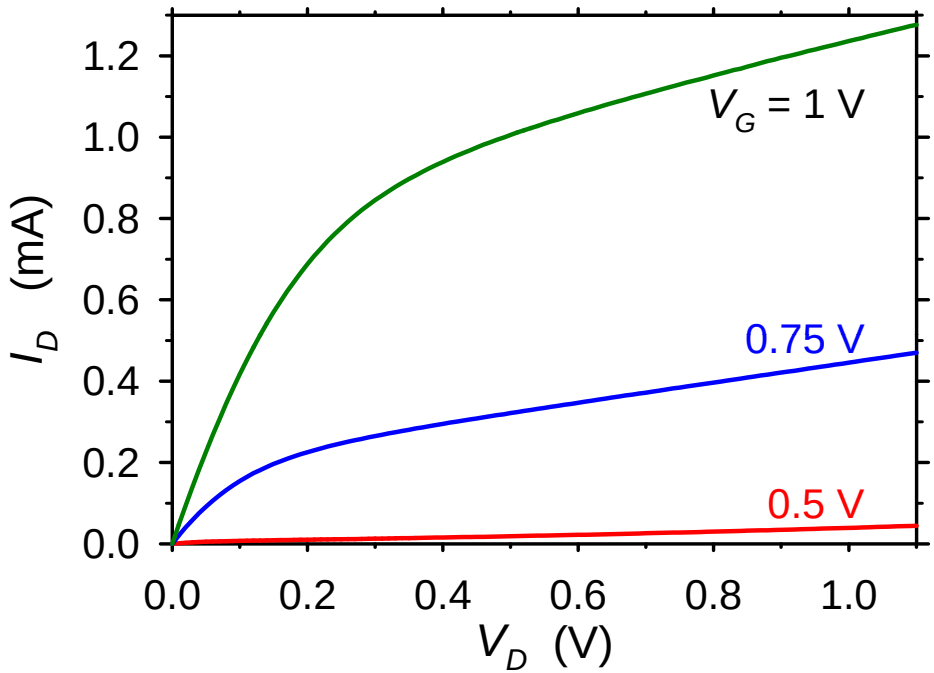
$$H_r\left(V_G\right) = \frac{\left[I_D - I_D\left(V_G = 0\right)\right]}{\int_0^{V_G} I_D(V_G)\, dV_G}$$

$$TCR = \frac{d \ \ln\left(\sqrt{I_D}\right)}{d V_G}$$

$$H_{r-sat}\left(V_g\right) = \frac{\left[\sqrt{I_D} - \sqrt{I_D\left(V_g = 0\right)}\right]}{\int_0^{V_g} \sqrt{I_D}\, dV_g}$$

2.12. Conductance method presented in a recent Chinese Patent [HE12; HU13]

It requires at least two output characteristics.



[HE12] He, Jin et al, "Threshold voltage extraction method for field effect transistors", Chinese patent: 201210153935. 2012-05-07.

[HU13] Yang Hui and Guo Yu-feng, "A Review of MOSFET Threshold Voltage Extraction Methods", College of Electronics Science & Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210003, P. R. China, Aug. 2013.

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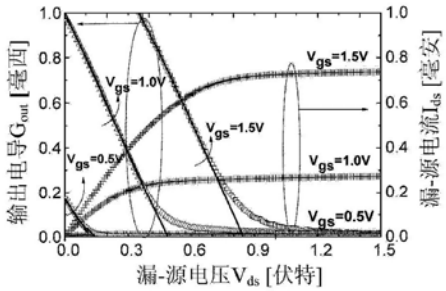
(51) Int.Cl.
G01R 31/30 (2006.01)

权利要求书 1 页 说明书 3 页 附图 2 页

(54) 发明名称
一种场效应晶体管阈值电压提取方法

(57) 摘要

本发明涉及一种尤其适用于纳米 FinFET 场效应晶体管的阈值电压提取方法，包括：选择三点不同漏－源电压 Vds，将栅－源电压 Vgs 从 -0.5 伏扫描到 +1.5 伏，测试出场效应晶体管的转移电流特性曲线 Ids-Vgs，确定器件正常工作；选择三点不同 Vgs，将 Vds 从 0 伏扫描到 +1.5 伏，测试出场效应晶体管的输出电流特性曲线 Ids-Vds；将漏－源输出电流 Ids 对 Vds 求导，得到输出电导特性曲线 Gout-Vds，再在线性区内选二点获取对应直线的截距和斜率；提取场效应晶体管的阈值电压 Vth，$V_{th}=\frac{V_{gs1}-(\eta_A/\eta_B)V_{gs2}}{(1-\eta_A/\eta_B)}$。这种方法实现简单，在低 Vds 下对偏置波动不敏感，能抑制小尺寸器件引起的短沟效应和超薄体效应。

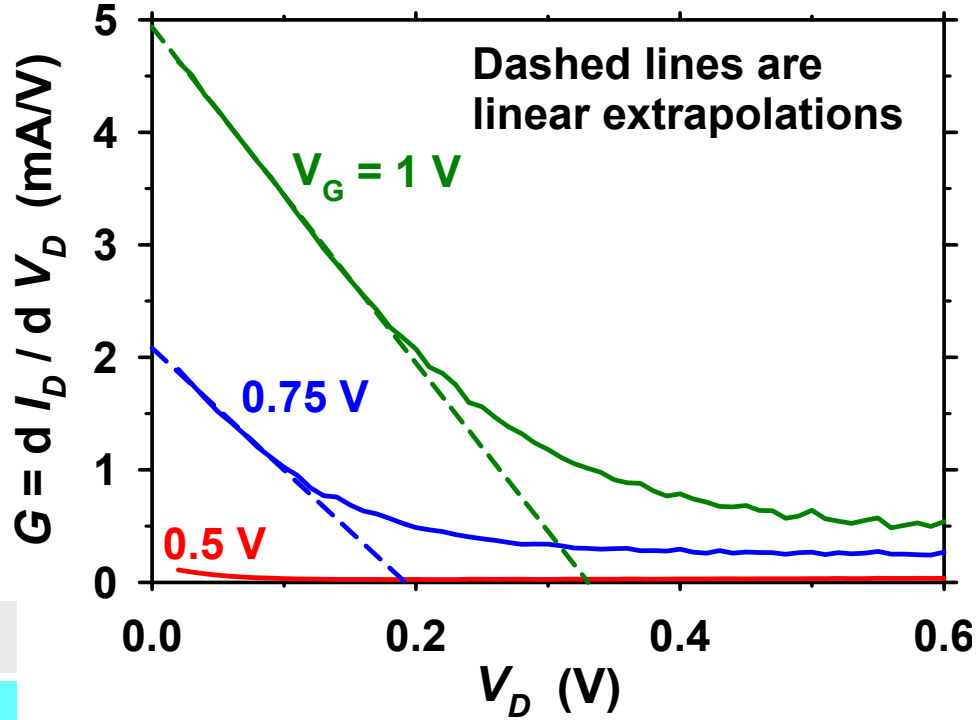


This method is based on:

$$I_D = \frac{W\,\mu_o C_o}{L(1+\theta V_G)}\left[V_G - V_G - \frac{V_D}{2}\right]V_D$$

First, we measure G. Then, we fit the following straight line to obtain A and B:

$$G = \frac{d\,I_D}{d\,V_D} = A - BV_D$$



V_G (V)	A (mA/V)	B (mA/V^2)
V_{G1} = 0.75	2.08	10.8
V_{G2} = 1	4.94	14.9

Evaluating: $\eta_a = \dfrac{A\big|_{V_G=V_{G1}}}{A\big|_{V_G=V_{G2}}} = \dfrac{2.08}{4.94} = 0.42$ $\quad \eta_b = \dfrac{B\big|_{V_G=V_{G1}}}{B\big|_{V_G=V_{G2}}} = \dfrac{10.8}{14.9} = 0.72$

$$V_T = \frac{\eta_b V_{G1} - \eta_a V_{G2}}{\eta_b - \eta_a} = 0.40V$$

This method yield to a low value of V_T.

2.13 Nonlinear optimization methods

2.13.1 The three-point direct extraction by Hamer [HA86]

$$I_D = K \frac{\left(V_G - V_T - \frac{V_D}{2} \right)}{1 + \theta \left(V_G - V_T \right)} V_D$$

can be transformed into

$$I_D = \frac{a + b V_G}{1 + c V_G}$$

where

$$a = -b \left(V_T + \frac{V_D}{2} \right)$$

$$b = \frac{K V_D}{1 - \theta V_T}$$

$$c = \frac{\theta}{1 - \theta V_T}$$

The parameters a, b, and c can be determined from three measurements or by fitting it to the complete data. Knowing a, b and c, the device parameters are evaluated by:

$$K = \frac{b}{\left(1 + c V_T\right) V_D}$$

$$V_T = -\frac{a}{b} - \frac{V_D}{2}$$

$$\theta = \frac{c}{1 + c V_T}$$

[HA86] Hamer, M.F. "First-order parameter extraction on enhancement silicon MOS transistors", 1986, IEE Proceedings I: Solid State and Electron Devices, 133 (2), pp. 49-54.

2.13.2 The four-point direct extraction by Karlsson and Jeppson [KA93;JE13]

$$I_D = K \frac{\left(V_G - V_T - \frac{V_D}{2}\right)}{1 + \theta_1 (V_G - V_T) + \theta_2 (V_G - V_T)^2} V_D$$

is transformed into

$$I_D = \frac{a + bV_G}{1 + cV_G + dV_G^2}$$

where $a = -b\left(V_T + \frac{V_D}{2}\right)$

$$b = \frac{KV_D}{1 - \theta_1 V_T + \theta_2 V_T^2}$$

$$c = \frac{\theta_1 - \theta_2 V_T}{1 - \theta_1 V_T + \theta_2 V_T^2}$$

$$d = \frac{\theta_2}{1 - \theta_1 V_T + \theta_2 V_T^2}$$

The parameters a, b, c and d can be determined from three measurements or by fitting it to the complete data.
Knowing a, b, c and d, the device parameters are evaluated by:

$$K = \frac{b}{\left(1 + cV_T + dV_T^2\right) V_D}$$

$$V_T = -\frac{a}{b} - \frac{V_D}{2}$$

$$\theta_1 = \frac{c + 2dV_T}{1 + cV_T + dV_T^2}$$

$$\theta_2 = \frac{d}{1 + cV_T + dV_T^2}$$

By setting $\theta_1 = \theta$ and $\theta_2 = 0$ (d=0), this method yield to the previous three-point method.

[KA93] Karlsson, P.R., Jeppson, K. O. "Direct extraction algorithm for a submicron MOS transistor model", (1993) IEEE International Conference on Microelectronic Test Structures, pp. 157-162.

[JE13] Jeppson, K.O."Three- and four-point Hamer-type MOSFET parameter extraction methods revisited", 2013, IEEE ICMTS , art. no. 6528161 , pp. 141-145.

The obtained fitting parameters are:

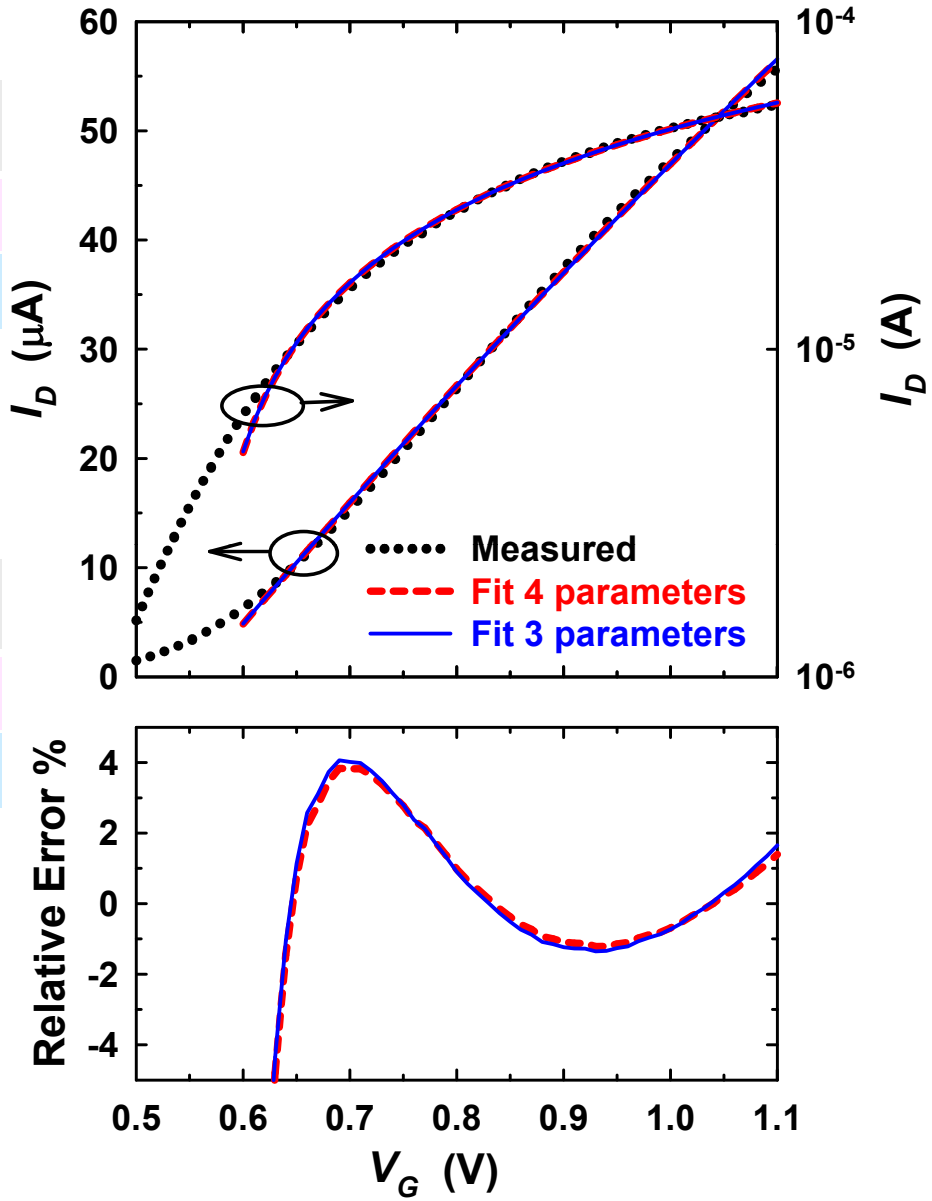
Number of Parameters	a (μA)	*b* (μA/V)	*c* (V^{-1})	*d* (V^{-2})
4	-65.31	117.23	5.3e-5	0.1053
3	-71.22	127.83	0.2055	

Then, the extracted parameters are:

Number of Parameters	V_T (V)	K (mA/V^2)	θ_1 (V^{-1})	θ_2 (V^{-2})
4	0.5521	11.4	0.1127	0.1020
3	0.5522	11.5	0.1845	

For this particular case, both models (3 and 4 parameters) yields approximately to the same reasonable results.

These methods require non-linear optimization.



Comparison of various threshold voltage methods 1/2

Method	V_T (V) in linear region (V_D = 10 mV)	V_T (V) in saturation region (V_D = 1.1 V)
Constant Current (CC)	0.57	0.45
Match-Point (MP)	0.35	0.31
Linear Extrapolation (LE)	0.57	0.41
Second Derivative (SD)	0.55	0.45
Third-derivative (TD)	0.48	NA*
Current-to-square-root-Transconductance Ratio (CsrTR) Linear by Jain and Ghibaudo (1988)	0.61	0.46
Current-to-square-root-Transconductance Ratio (CsrTR) by us using empirical model (2013)	0.55	NA*
Current-to-square-root-Transconductance Ratio (CsrTR) by Tsormpatzoglou (2012)	0.59	NA*

*NA means Not Applicable

Comparison of various threshold voltage methods 2/2

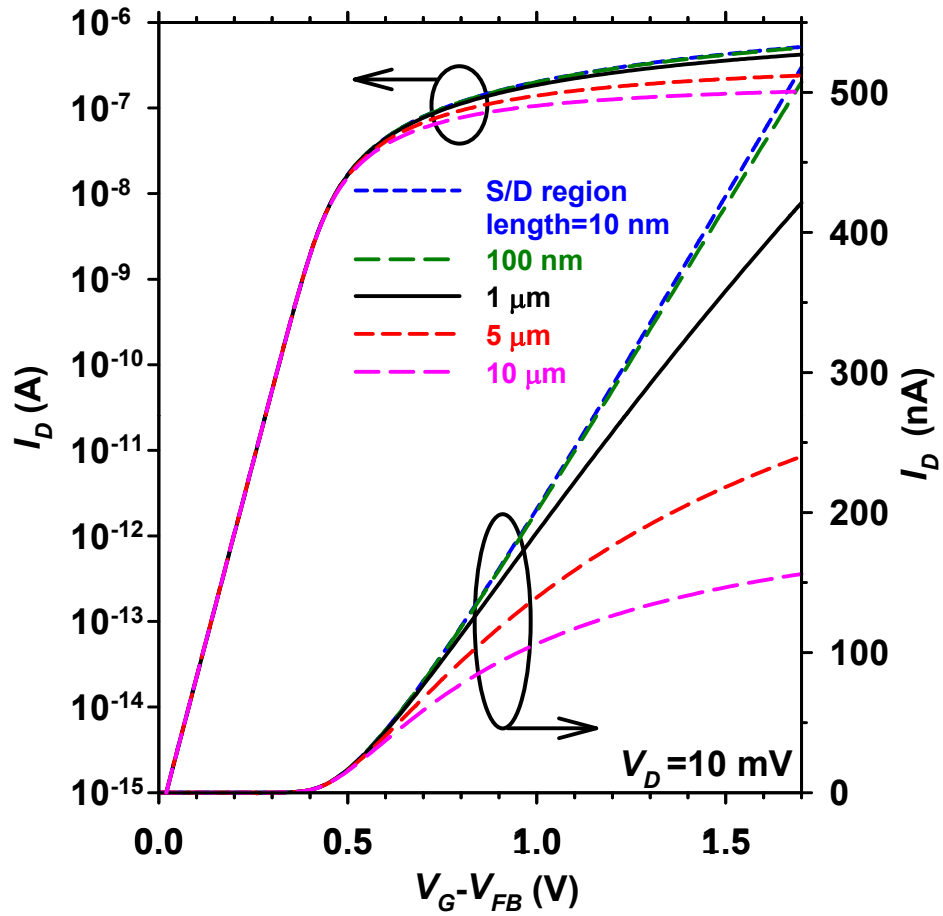
Method	V_T (V) in linear region (V_D = 10 mV)	V_T (V) in saturation region (V_D = 1.1 V)
Transition	0.54	0.37
Normalized Mutual Integral Difference (NMID)	0.46	0.47
Normalized Reciprocal H (NRH)	0.46	0.47
SDL by Aoyama (1995) or TCR at Maximum slope by Flandre (2010)	0.53	0.44
TCR at (1/2) TCR_{max} by Cunha (2005)	0.56	NA*
TCR at (2/3) TCR_{max} by Rudenko (2011)	0.49	NA*
Reciprocal H (RH)	0.55	0.52
Conductance method presented in a recent Chinese Patent	0.40	NA*
Nonlinear optimization methods	0.55	NA*

*NA means Not Applicable

3. 2-D simulations for several S/D regions length

Increasing S/D regions' length is equivalent to *increasing the series resistance*.

Simulations of an undoped DG MOSFET (V_{FB}=-1.03V) , using the "MOSFet" tool [MA12], were carried out with constant mobility and S/D regions length varying from 10 nm to 10 μm.
Other used parameters were: *n*+ polysilicon gate, S/D with doping concentrations of 10^{18} cm^{-3}, a body doping concentrations of 10^{12} cm^{-3} and a 100-μm channel length.



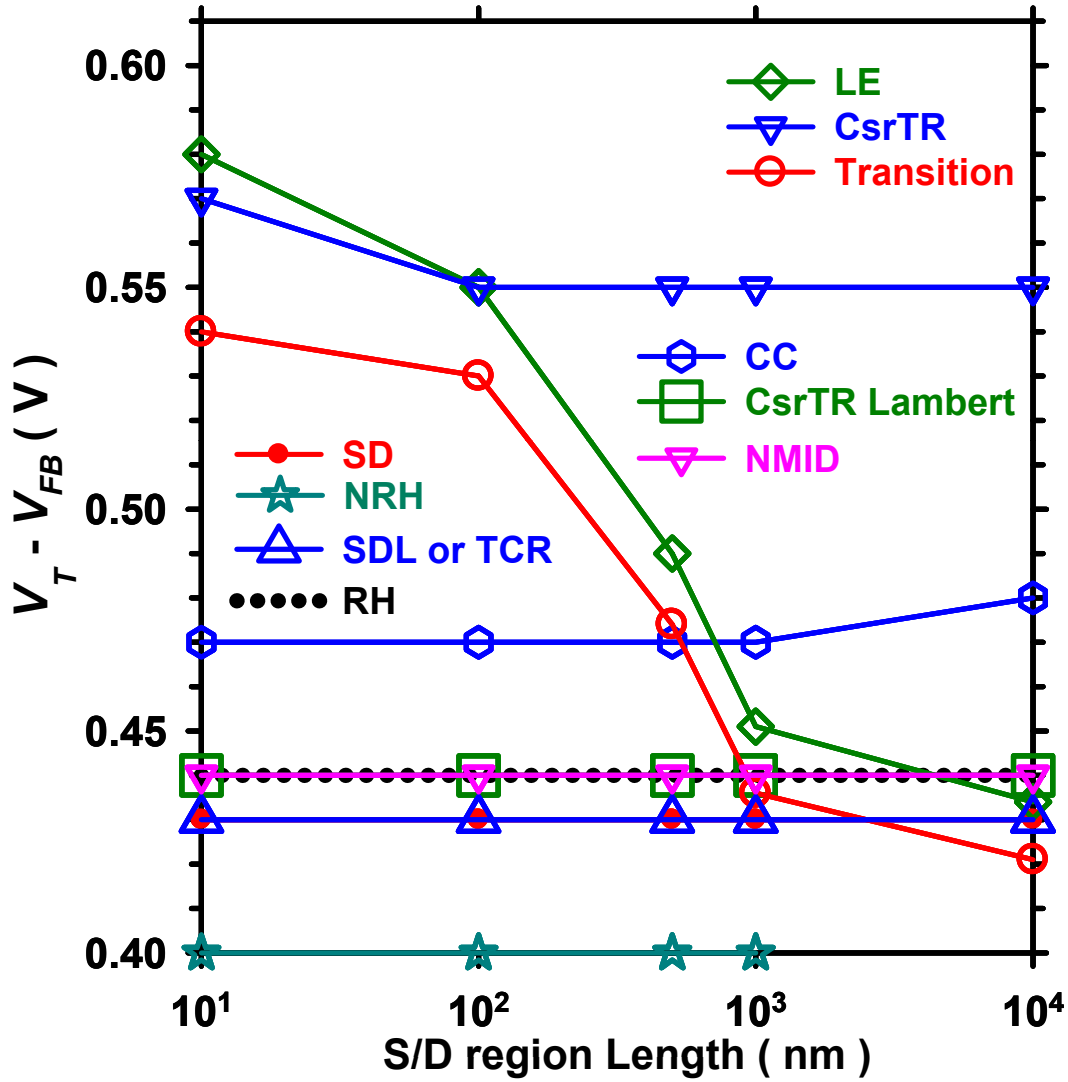
[MA12] M. Mannino, S. S. Ahmed, G. Klimeck, D. Vasileska, X. Wang, H. Pal, S. R. Mehrotra, and G. W. Budiman, MOSFet, 2012, DOI: 10254/nanohub-r452.18..

V_T versus S/D regions length

LE and Transition methods depend strongly on series resistance.

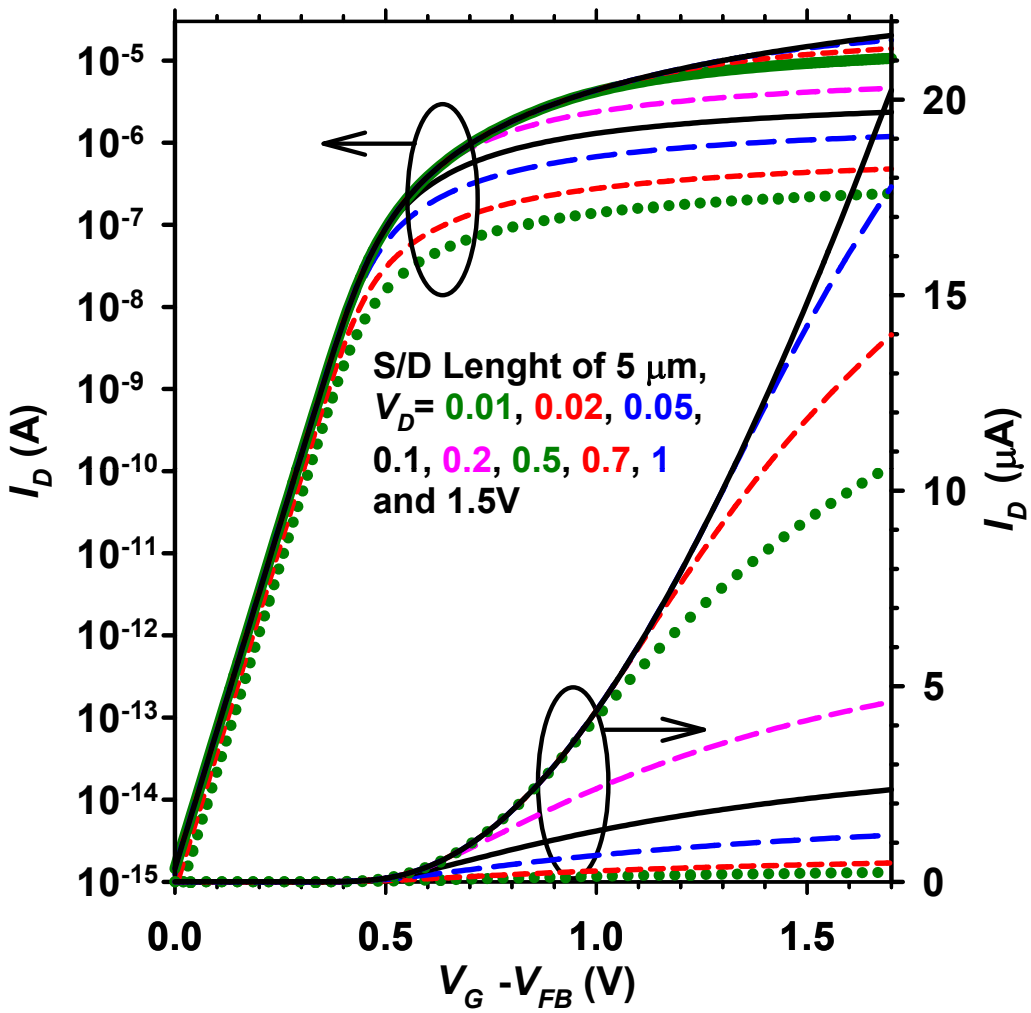
CsrTR, CC and NRH methods are weakly dependent on series resistance.

SD, SDL, NMID, RH, and CsrTR Lambert methods do not dependend on series resistance.



Transfer characteristics 2-D simulations for different values of drain voltage

Simulations of $I_D(V_G)$ with several values of V_D for an undoped DG MOSFET, using the "MOSFet" tool [MA12] , were carried out with a S/D regions length of 5 μm.



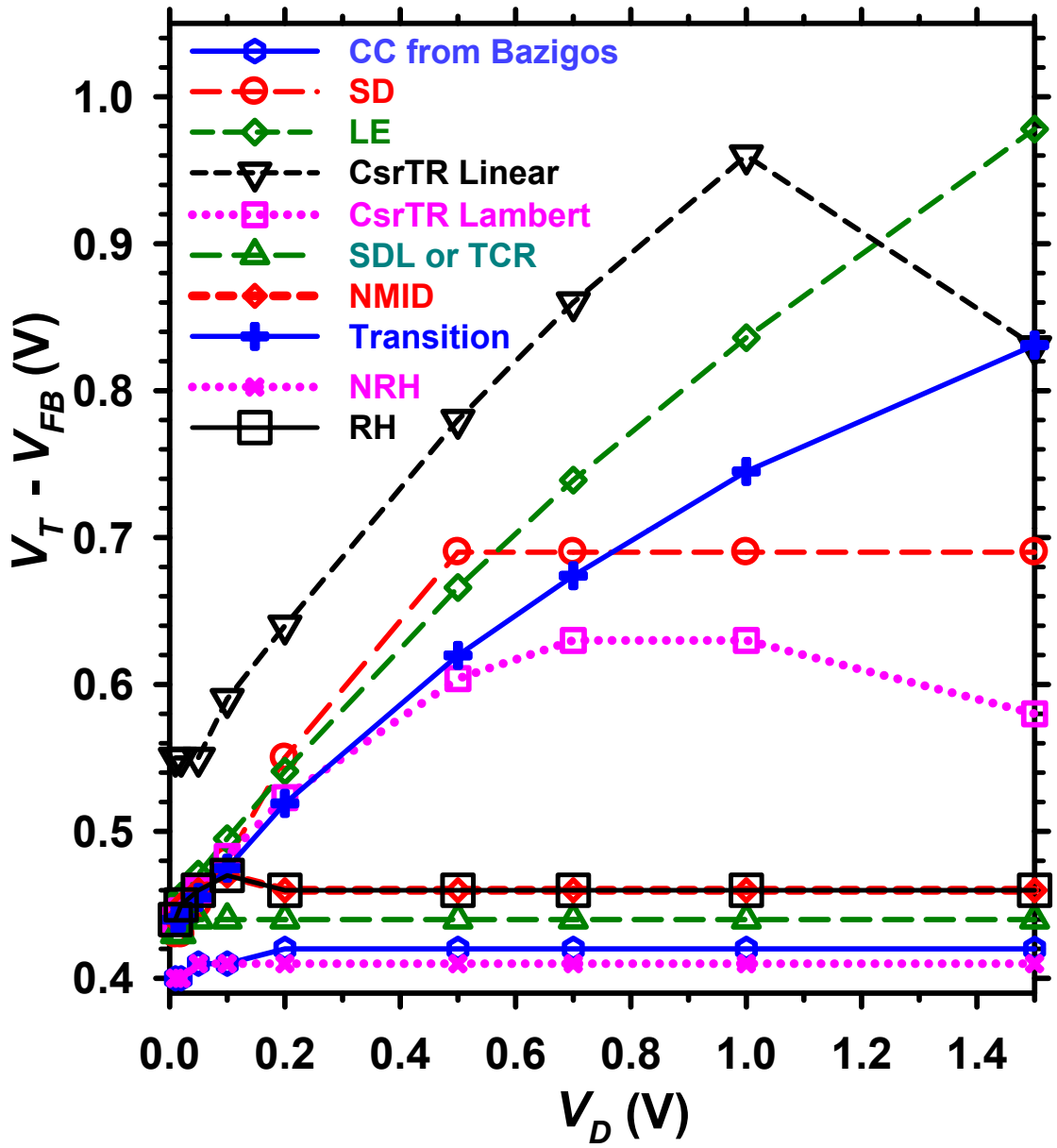
[MA12] M. Mannino, S. S. Ahmed, G. Klimeck, D. Vasileska, X. Wang, H. Pal, S. R. Mehrotra, and G. W. Budiman, MOSFet, 2012, DOI: 10254/nanohub-r452.18..

V_T versus V_D

LE, CsrTR, and Transition methods depend strongly on drain voltage.

SD and CsrTR Lambert methods are weakly dependent on drain voltage.

SDL, NMID, CC (from Bazigos), NRH and RH methods do not dependent on drain voltage.



4. V_T extraction for non-crystalline MOSFETs

The weak inversion current (I_{Dw}) is modeled by:

$$I_{Dw} = I_o \exp\left(\frac{V_G}{n v_{th}}\right)$$

where I_0 is a global coefficient and n is the subthreshold ideality factor.

The strong inversion current (I_{Ds}) , at low drain voltage, exhibit a monomial type equation:

$$I_{Ds} = K\left(V_G - V_{Ts}\right)^m V_D$$

where *K* is a global conduction coefficient, *m* is the monomial's order, usually around 2, and V_{Ts} is the I_{Ds}=0 intercept, which can be viewed as a "strong inversion region-defined" threshold voltage.

There are two recent review articles about integration-based parameter extraction methods: for MOSFET [OR08] and for two-terminal devices [GAO8].

[GA08] F.J. García Sánchez, A. Ortiz-Conde, and G. De Mercato, "The Development of Integration-based Methods to Extract Parameters of Two-Terminal Device Models", The 9th Int. Conf. on Solid-State and Int.-Circuit Tech. (ICSICT) Beijing, pp. 432-435, Oct. 2008.
[OR08] A. Ortiz-Conde, F.J. García Sánchez, and R. Salazar, "On Integration-based Methods for MOSFET Model Parameter Extraction (Invited)", The 9th Int. Conf. on Solid-State and Integrated-Circuit Technology (ICSICT) Beijing, China, pp. 428- 431, Oct. 2008.

4.1. Single Integration method: H_1 function

An integration-based method was proposed in 2001 for extracting model parameters of non-crystalline MOSFETs biased in the saturation region [OR01].

The auxiliary function used in that method had been originally proposed in 1999 by our group to extract the model parameters of PN junctions at very low forward voltages [RA99].

The auxiliary function has the form:

$$H_1(I_D, V_G) = \frac{\int_{VGlow}^{VG} I_D(V_G)\, dV_G}{I_D - I_{low}}$$

where $I_{low} = I_D(V_G = V_{G\,low})$, and V_{Glow} is the lower limit of integration.

[OR01] Ortiz-Conde A, Cerdeira A, Estrada M, García Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. Solid-State Electronics 2001; 45: 663-667.

[RA99] J.C. Ranuarez, F.J. García-Sánchez, A. Ortiz-Conde, Procedure for the determination of diode model parameters at very low forward voltage, Solid-St. Electron., 43, 2129-2133 (1999).

For weak inversion:

$$I_{Dw} = I_o \exp\left(\frac{V_G}{n v_{th}}\right)$$

$$\Rightarrow \quad H_{1w}(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G}{I_D - I_{low}} = \frac{n v_{th} I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1\right]}{I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1\right]} = n v_{th}$$

which allows to extract *n* from a constant value.

For strong inversion:

$$I_{Ds} = K\left(V_G - V_{Ts}\right)^m V_D \quad \Rightarrow \quad H_{1s}(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G}{I_D - I_{low}} = \frac{V_G - V_{Ts}}{m+1}$$

which allows to extract *m* and V_{Ts} from an straight line.

The use of H_1 is an improvement over derivative-based methods regarding data noise reduction.

However, because H_1 still contains the possibly noisy raw current data in the denominator, it was proposed the use of a double integration method to further improve the noise immunity of the procedure.

4.2. Double Integration method: H_2 function

The previous idea was taken one step further with the purpose of reducing even more the effect of data noise. Function, H_2, based on successive double integration, was proposed [OR10b]:

$$H_2(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G\, dV_G}{\int_{V_{Glow}}^{V_G} \left[I_D(V_G) - I_D(V_G = V_{Glow}) \right] dV_G}$$

$$= \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G\, dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G - I_{low} V_G}$$

[OR10b] A. Ortiz-Conde, A. D Latorre Rey, W. Liu, W.-C. Chen, H.-C. Lin, J. J. Liou, J. Muci, F. J. García Sánchez, "Parameter extraction in polysilicon nanowire MOSFETs using new double integration-based procedure", Solid State Electronics. Vol. 54, pp. 635– 641, 2010.

For weak inversion: $I_{Dw} = I_o \exp\left(\frac{Vg}{n v_{th}}\right)$

$$H_{2w}(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G\, dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G - I_{low} V_G} = \frac{n v_{th} I_{low} \left\{ n v_{th} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - V_G \right\}}{n v_{th} I_{low} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - I_{low} V_G} = n v_{th}$$

which allows to extract *n* from a constant value.

For strong inversion: $I_{Ds} = K\left(V_G - V_{Ts}\right)^m V_D$

$$H_{2s}(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G\, dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G)\, dV_G - I_{low} V_G} = \frac{V_G - V_{Ts}}{m+2}$$

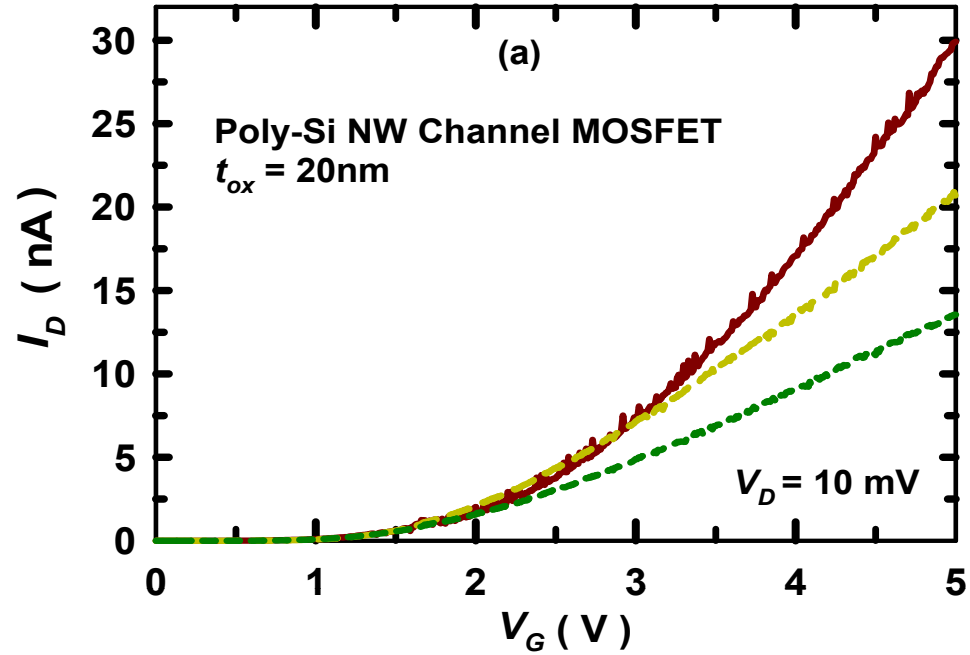
which allows to extract *m* and V_{Ts} from an straight line.

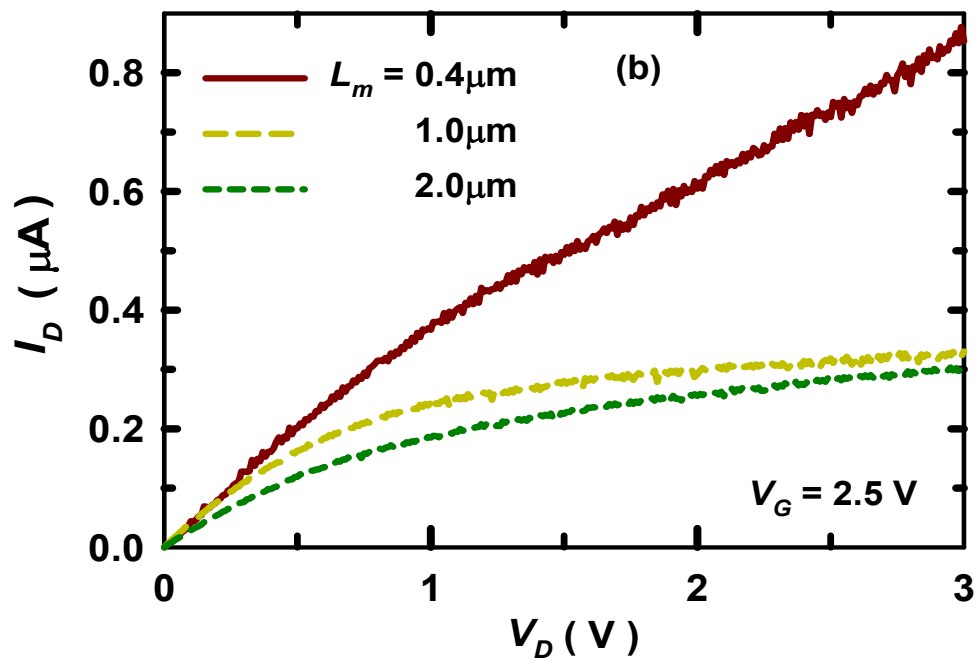
The use of H_2 is an improvement with respect to H_1 regarding data noise reduction.

Both procedures were applied to a polycrystalline silicon nanowire n-channel MOSFETs, fabricated at the National Chiao Tung University, Hsinchu, Taiwan.

They were later measured at the University of Central Florida, Orlando FL, USA.

Three devices with the following makeup were used: Undoped poly-Si NW body with a rectangular cross section of 60nm x 18nm, channel lengths of 0.4, 1.0, and 2.0 mm, n^+ polysilicon gate with 10^{21} cm^{-3} doping, gate SiO_2 oxide thickness of 20nm, and S/D doping density of $5x10^{20}$ cm^{-3}.



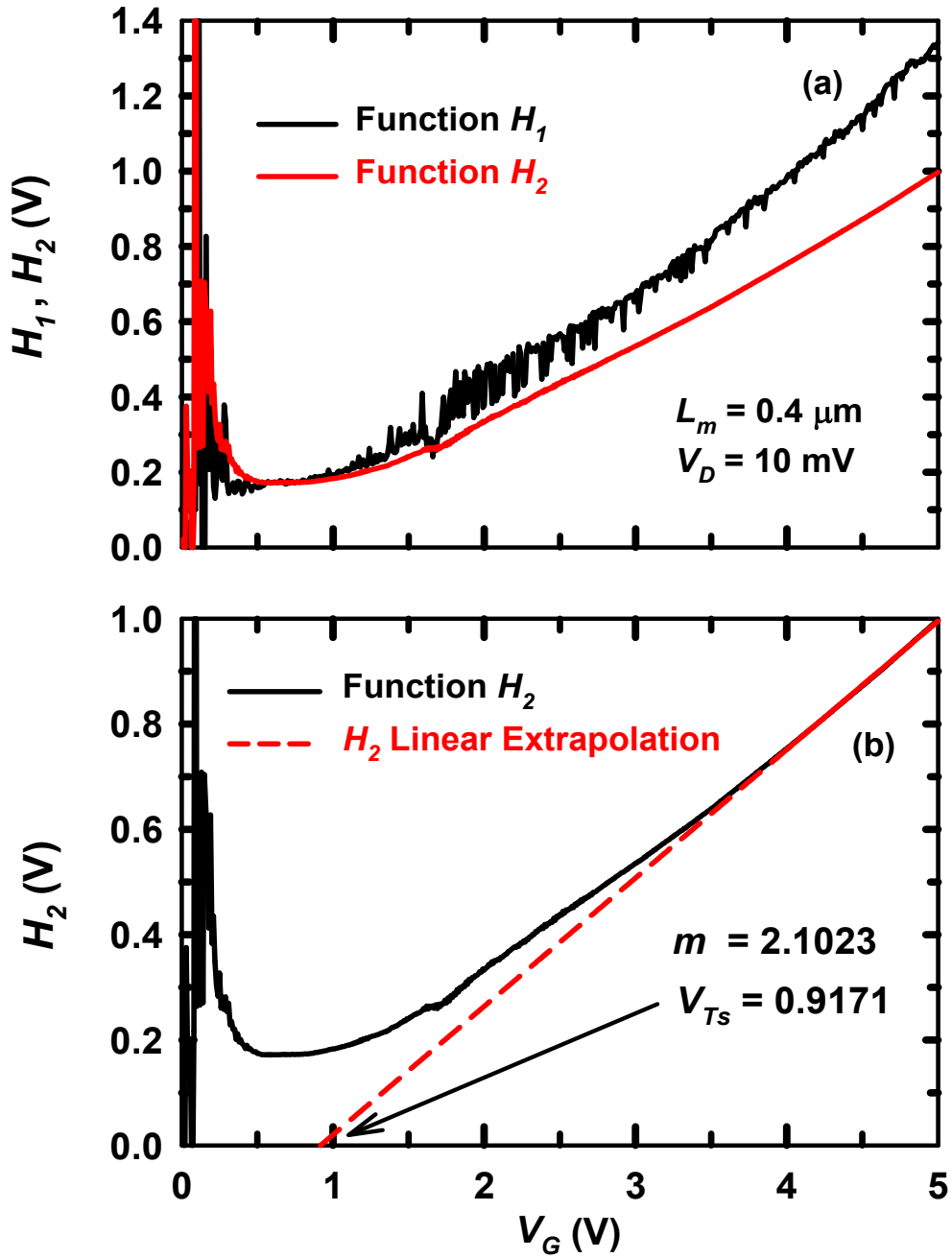


In weak inversion, H_1 and H_2 approximate the same value of nv_{th} .

H_2 is less noisy then H_1.

In strong inversion, H_1 and H_2 tends to be straight lines with slopes 1/(m+1) and 1/(m+2) respectively.

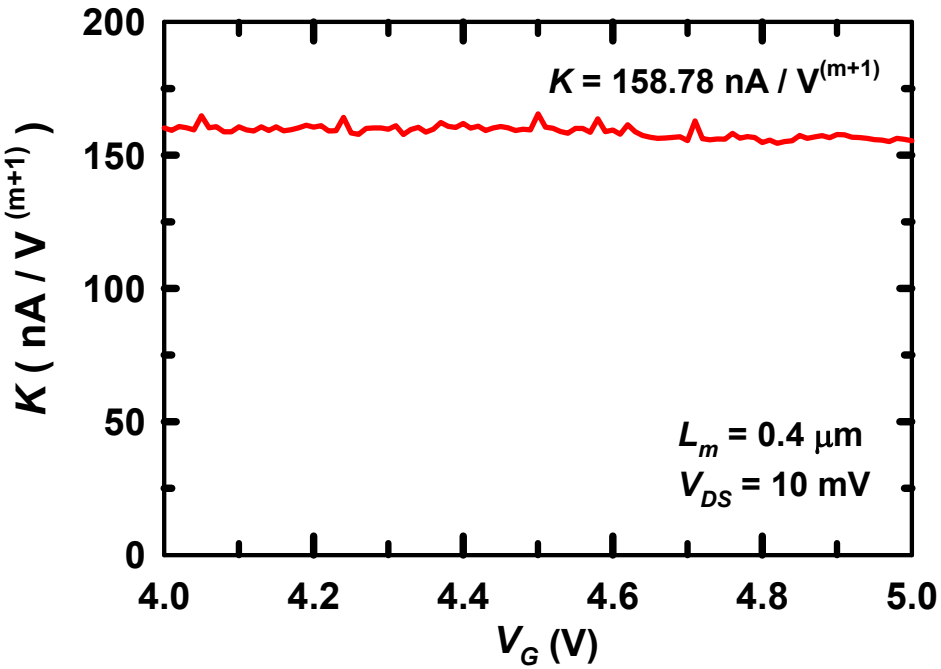
The values extracted from the straight line are m = 2.1023, and V_{Ts} = 0.92 V .



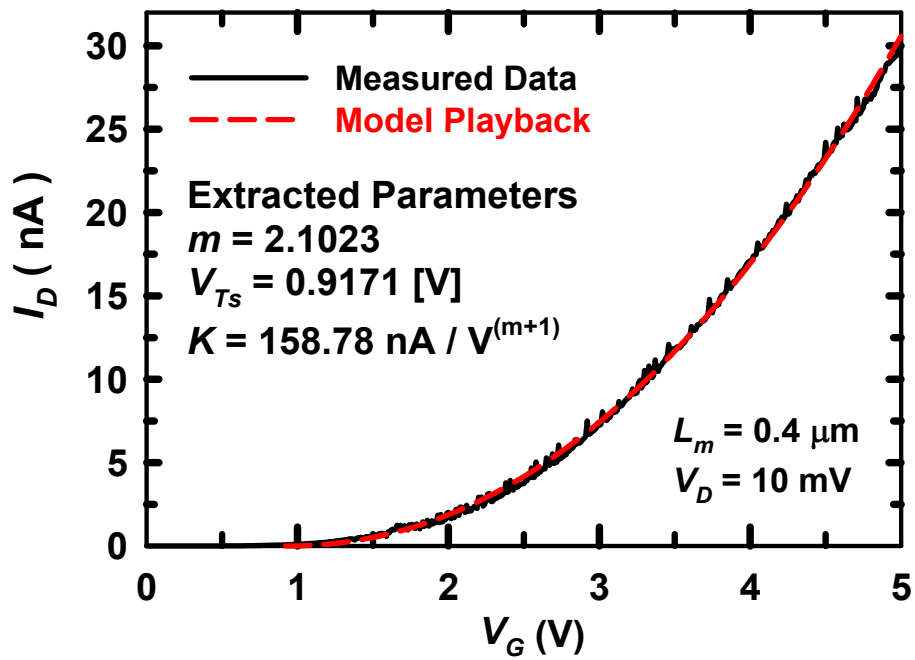
Knowing the values of *m* and V_{Ts} from the linear fit, we calculate K by using:

$$K = \frac{I_{Ds}}{\left(V_G - V_{Ts}\right)^m V_D}$$

***K* looks fairly constant at a mean value of *K* = 158.78 nA / V$^{(m+1)}$, for the chosen V_G range.**



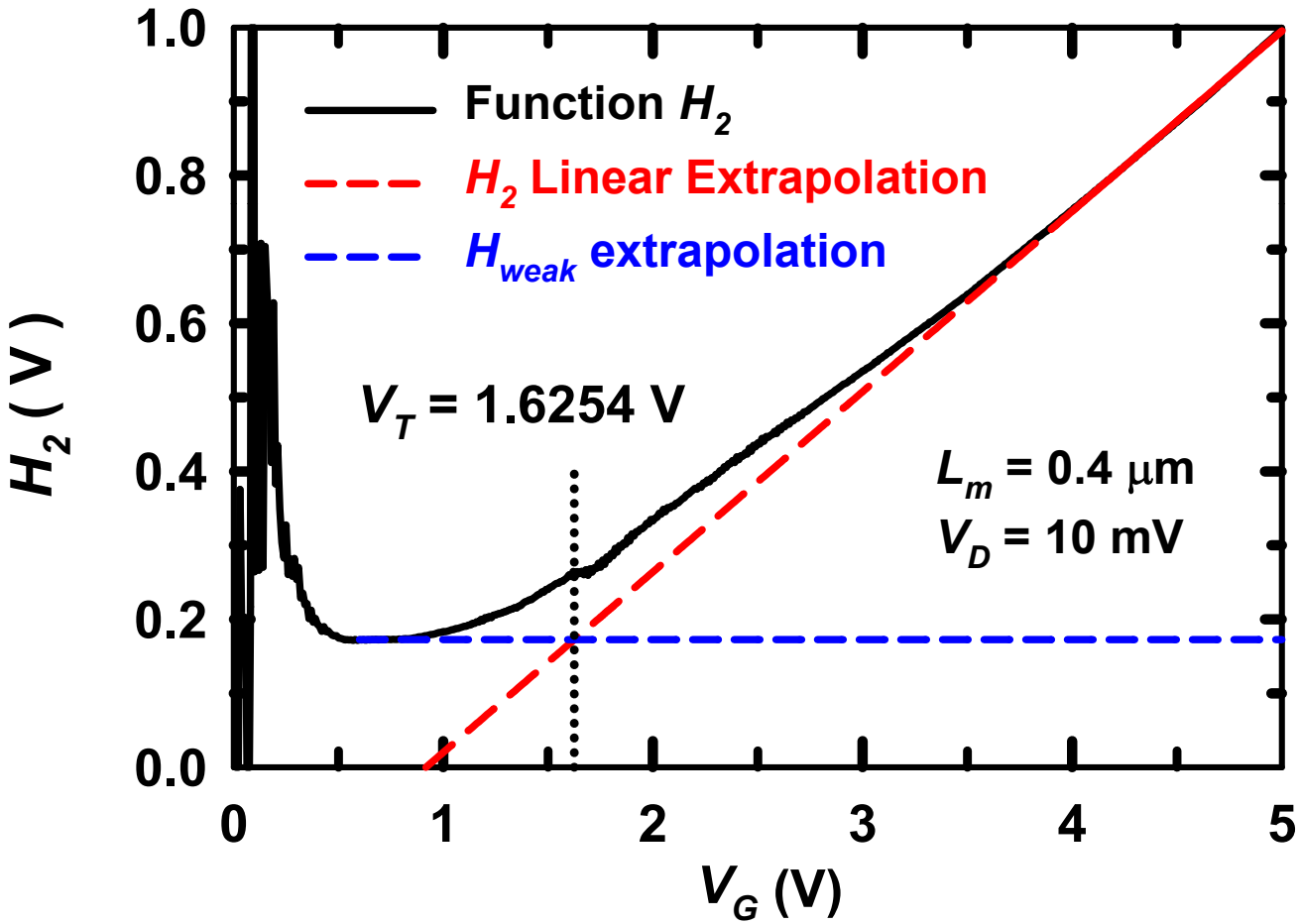
As a confirmation, we present the measured transfer characteristic together with the model playback.



Phenomenological threshold voltage

Finally, the phenomenological threshold voltage V_T is obtained as the value of V_G where H_{weak} intersects the linear extrapolation of the strong inversion region of H_2 (H_{2S}).

A value of V_T = 1.63 V is the result for this device.



4.3. Recent Derivative method for organic transistors [SI13]

For strong conduction:

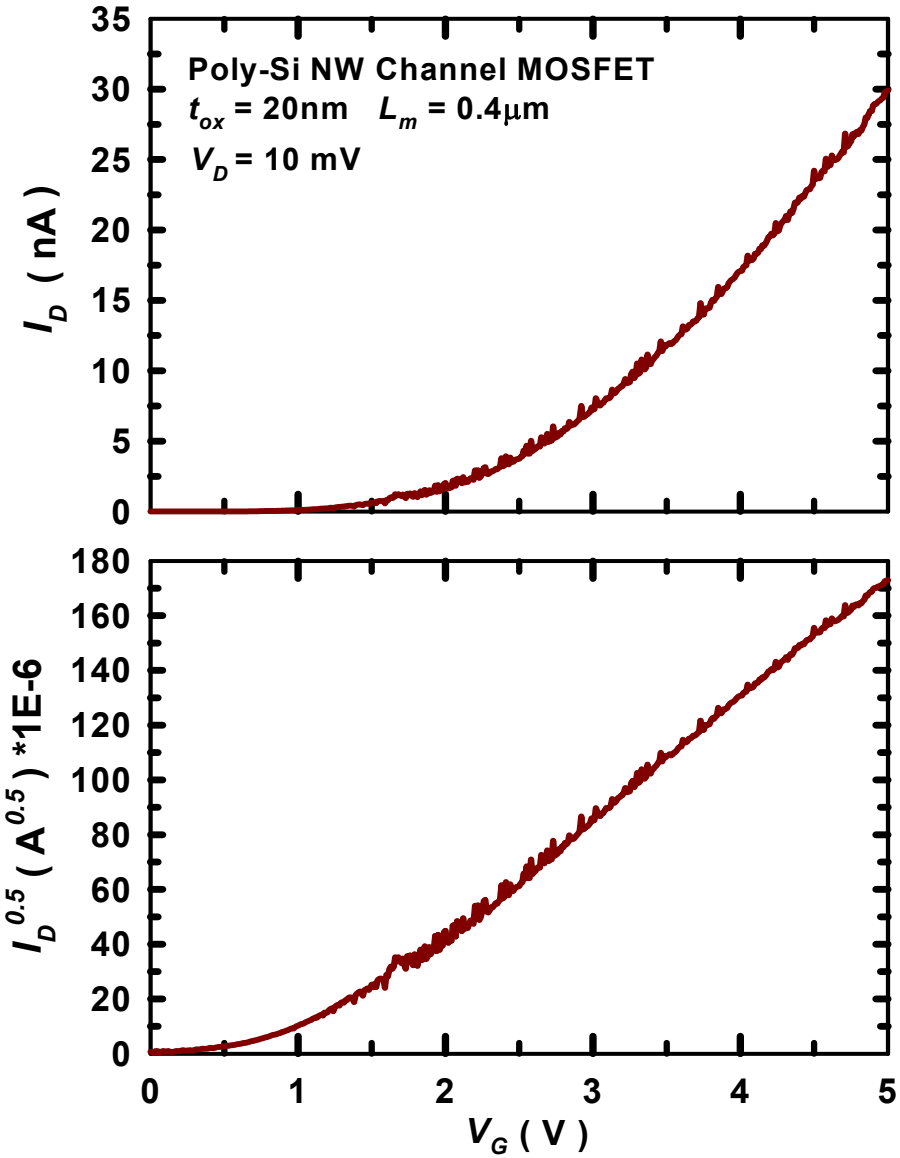
$$I_D = K\left(V_G - V_T\right)^m$$

Using LE method for $I_D^{0.5}$, at an arbitrary value of gate bias V_{Gx} :

$$V_{T-LE} = V_{Gx} - \left[\frac{\sqrt{I_D}}{\frac{d\sqrt{I_D}}{dV_G}}\right]_{V_G = V_{Gx}}$$

The previous equation is evaluated using experimental data. Finally, V_T and *m are* extracted using the following equation:

$$V_{T-LE} = \left(1 - \frac{2}{m}\right)V_{Gx} - \frac{2}{m}V_T$$



[SI13] Kumar Singh, V., Mazhari, B., "Measurement of threshold voltage in organic thin film transistors", Applied Physics Letters 102 (25) , art. no. 253304, 24 June 2013.

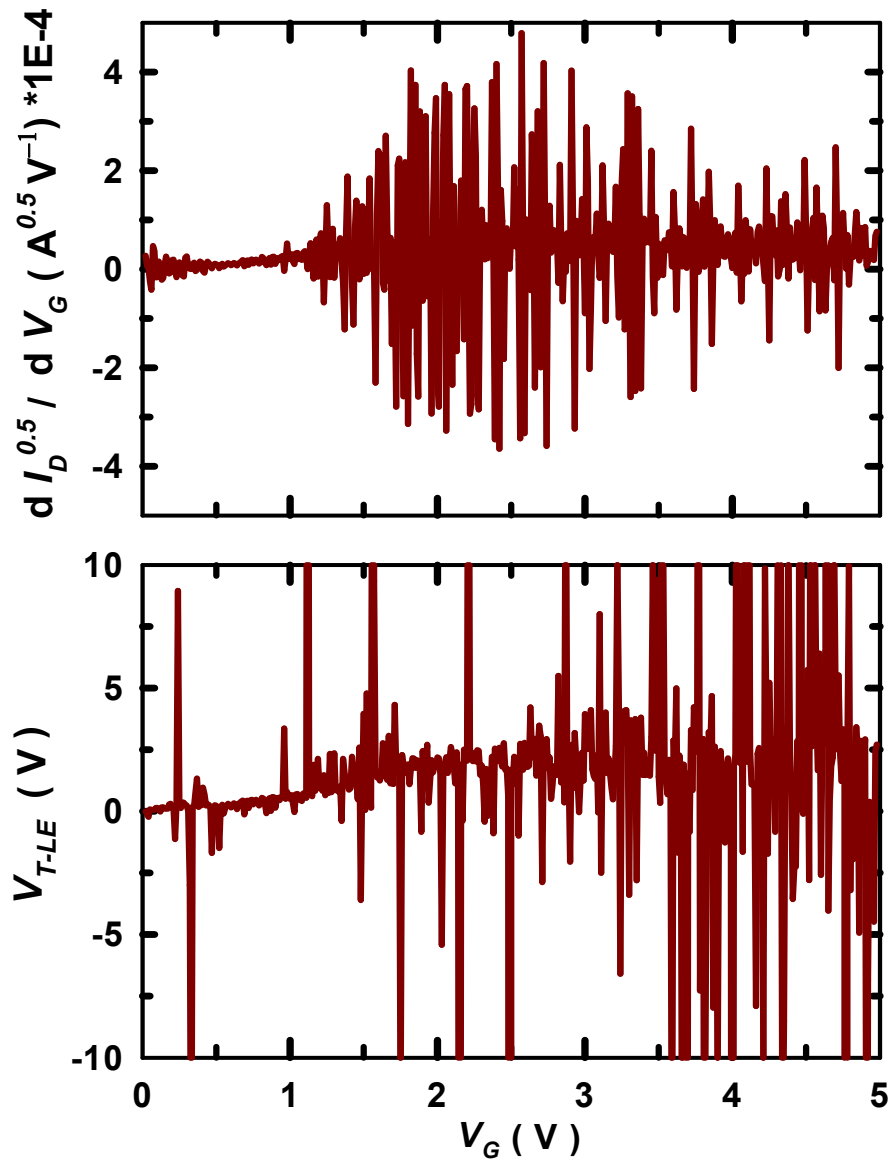
We observe that this derivative is too noisy: $\dfrac{d\sqrt{I_D}}{dV_G}$

$V_{T\text{-}LE}$ is useless because of the high experimental noise.

$$V_{T-LE} = V_{Gx} - \left[\frac{\sqrt{I_D}}{\dfrac{d\sqrt{I_D}}{dV_G}} \right]_{V_G = V_{Gx}}$$

It is not possible to see the expected straight line:

$$V_{T-LE} = \left(1 - \frac{2}{m}\right) V_{Gx} - \frac{2}{m} V_T$$



5. V_T extraction from small signal high frequency measurements

MOSFET's model for high-frequency generally requires parameter extraction first in DC and then in high frequency.

Errors in the DC extraction procedure will produce errors in the high frequency parameters.

Álvarez-Botero et al [AL11] recently proposed to obtain all the parameters from the high frequency measurements.

[AL11] Álvarez-Botero, G., Torres-Torres, R., Murphy-Arteaga, R., "Using S-parameter measurements to determine the threshold voltage, gain factor, and mobility degradation factor for microwave bulk-MOSFETs", Microelectronics Reliability 51 (2) , pp. 342-349, 2011.

5.1. Conductance-to-square-root-Conductance's derivative-Ratio (CsrCdR) method

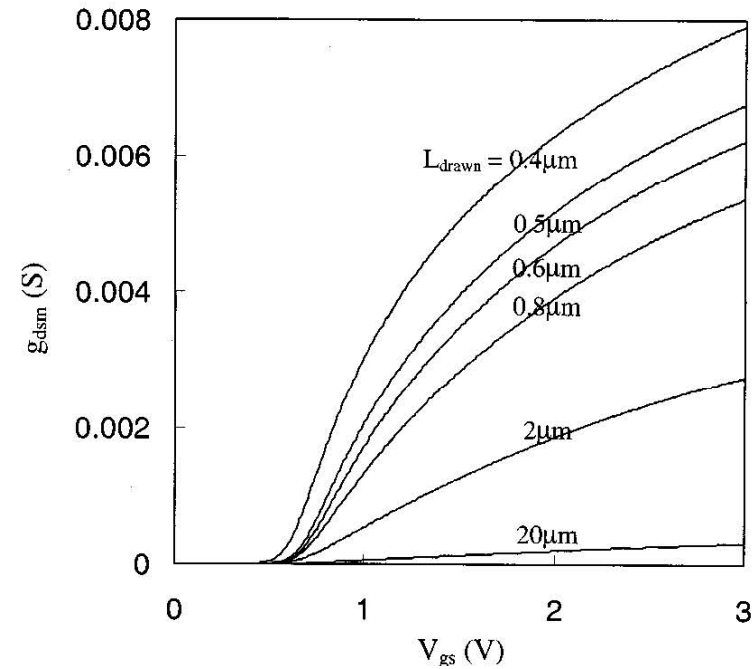
Kong et al proposed in 2001 [KO01] the following function:

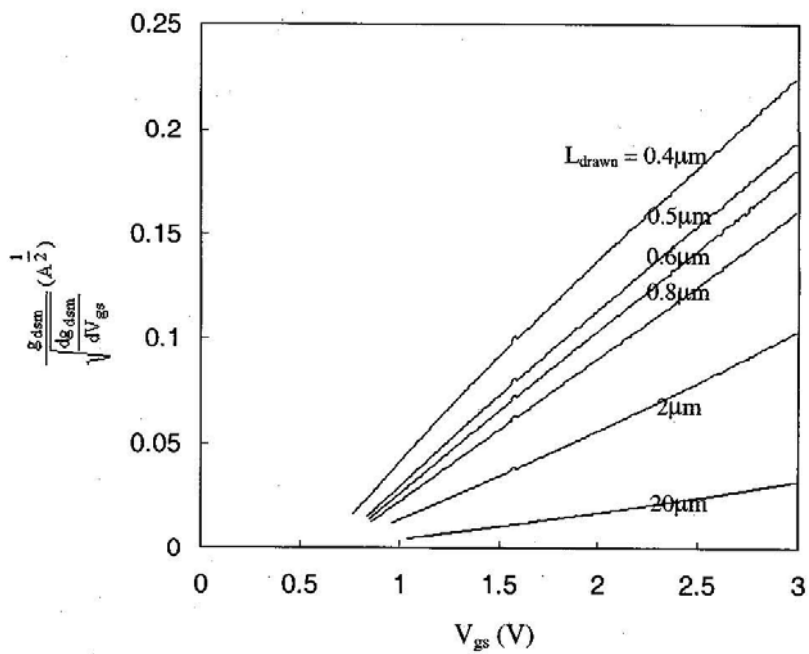
$$CsrCdR \equiv \frac{g_{dsm}}{\sqrt{dg_{dsm}/dV_G}} = \beta^{1/2}\left(V_G - V_T \right)$$

where g_{dsm} is the measured small signal conductance and

$$\beta \equiv \frac{W}{L}\mu Co$$

CsrCdR is linear with V_G for strong inversion and its extrapolation to CsrCdR=0 yields to V_T .





[KO01] Kong, F.C.J., Yeow, Y.T., Yao, Z.Q., "Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small-signal channel conductance measurement", IEEE Transactions on Electron Devices 48 (12) , pp. 2870-2874, 2001.

This method (CsrCdR), developed in 2001, seems to be inspired in the previous Current-to-square-root-Transconductance Ratio (CsrTR) method, proposed in 1988 [JA88; GH88]:

$$CsrTR \equiv \frac{I_D}{\sqrt{dI_D/dV_G}} = s^{-1/2}\left(V_G - V_T\right)$$

We note that by replacing I_D by g_{dsm} in the previous equation (CsrTR) we obtain the definition of CsrCdR :

$$CsrCdR \equiv \frac{g_{dsm}}{\sqrt{dg_{dsm}/dV_G}} = \beta^{1/2}\left(V_G - V_T\right)$$

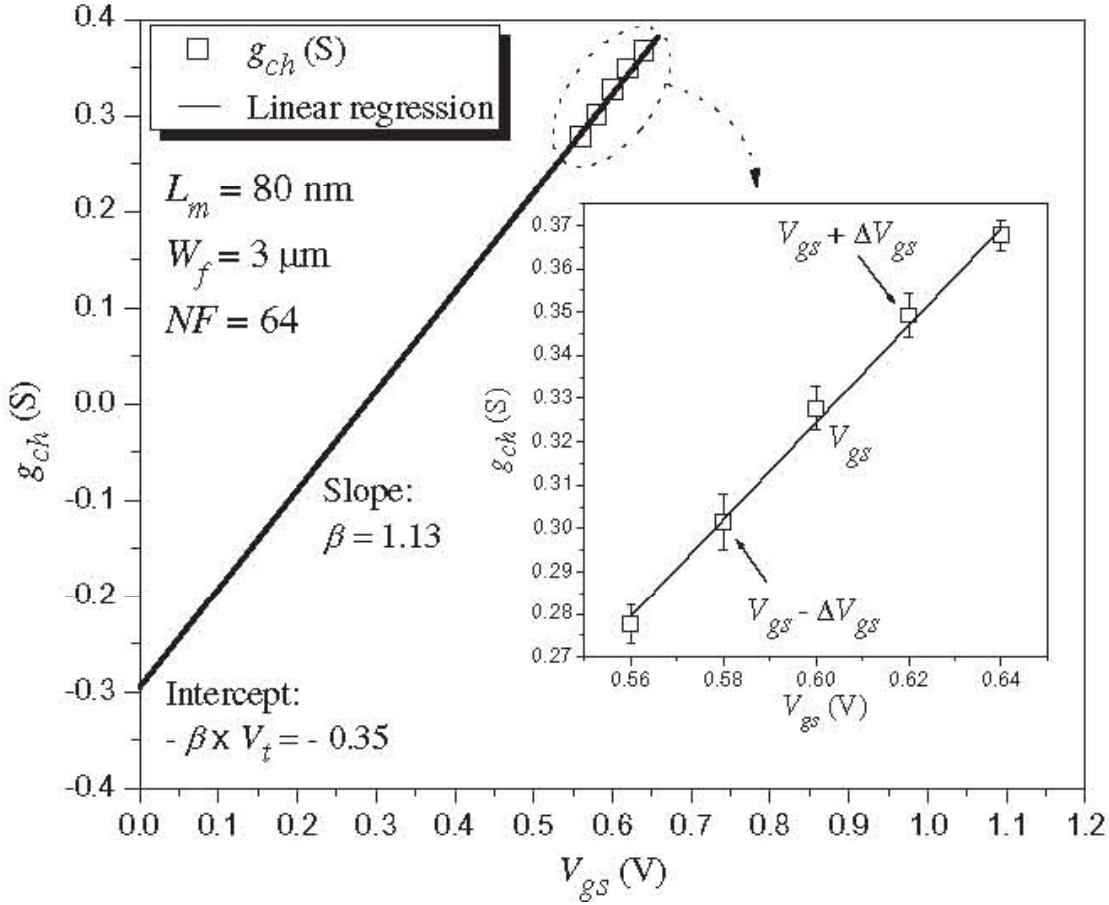
[JA88] Jain S. Measurement of threshold voltage and channel length of submicron MOSFETs." IEE Proc. Cir. Dev. and Sys. 1988; 135: 162.
[GH88] Ghibaudo G. New method for the extraction of MOSFET parameters. Electronics Letters 1988; 24: 543–545.

5.2. Linear extrapolation of the intrinsic small-signal drain-source conductance (LESSC)

Álvarez-Botero et al [AL11] recently proposed to obtain all the parameters from the high frequency measurements. Then, the intrinsic small-signal conductance between source and drain (g_{ch}) at V_{ds} = 0 is:

$$g_{ch} = \beta \left(V_G - V_T \right)$$

g_{ch} is linear with V_G and its extrapolation to g_{ch} =0 yields to V_T .



[AL11] Álvarez-Botero, G., Torres-Torres, R., Murphy-Arteaga, R., "Using S-parameter measurements to determine the threshold voltage, gain factor, and mobility degradation factor for microwave bulk-MOSFETs", Microelectronics Reliability 51 (2) , pp. 342-349, 2011.

Conclusions

- **We have presented, reviewed and critically compared several extraction methods used to determine the threshold voltage for crystalline and non-crystalline MOSFETs.**
- **The methods were compared under the same conditions by applying them to:**

(a) Measured characteristics of a crystalline MOSFET with state-of-the-art 65 nm channel length;

(b) 2D simulations of a Double-Gate MOSFET; and

(c) Measured characteristics of a polysilicon nanowire n-channel MOSFETs.

- **The simulations have allowed to evaluate the methods under the presence of significant series resistance and several drain voltages.**
- **As a result of scrutinizing the methods, variations and improvements have been proposed.**

END of presentation

Thank you for your attention

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Universidad Simón Bolívar
Caracas, Venezuela

Idea Transition Method_piecewise-v22.mws 3-Aug2012

Idea Transition
Method_piecewise-v22.mws 3Aug2012

```
> restart:  Digits:=20: with(plots):
> ID:=piecewise( VG<VT, ILeak, VG>=VT,
  K*(VG-VT)+ILeak) ;
```

$$ID := \begin{cases} ILeak & VG < VT \\ K\,(VG - VT) + ILeak & VT \le VG \end{cases}$$

```
> inte:=int(ID,VG);
```

$$inte := \begin{cases} ILeak\,VG & VG \le VT \\ K\left(\frac{1}{2}\,VG^2 - VT\,VG\right) + ILeak\,VG + \frac{K\,VT^2}{2} & VT < VG \end{cases}$$

```
> G1:= VG-2*inte/ID;
```

$$G1 := VG - \frac{2\left(\begin{cases} ILeak\,VG & VG \le VT \\ K\left(\frac{1}{2}\,VG^2 - VT\,VG\right) + ILeak\,VG + \frac{K\,VT^2}{2} & VT < VG \end{cases}\right)}{\begin{cases} ILeak & VG < VT \\ K\,(VG - VT) + ILeak & VT \le VG \end{cases}}$$

```
> G1weak:= VG - 2*(ILeak*VG)/ILeak;
```

$$G1weak := -VG$$

```
> G1strong:= VG -
  2*((K*(1/2*VG^2-VT*VG))+ILeak*VG+1/2*K*VT^2
  )/(K*(VG-VT)+ILeak);
```

$$G1strong := VG - \frac{2\left(K\left(\frac{1}{2}\,VG^2 - VT\,VG\right) + ILeak\,VG + \frac{K\,VT^2}{2}\right)}{K\,(VG - VT) + ILeak}$$

```
> limit(G1strong, ILeak=0);
```

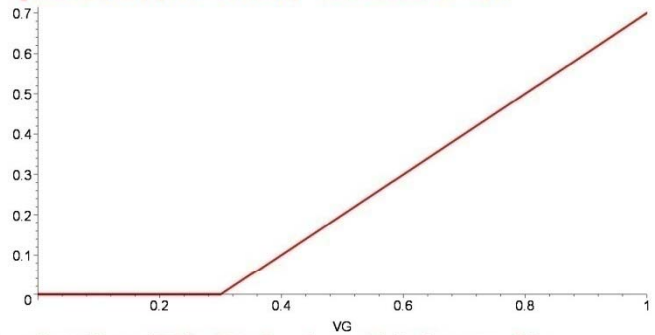
$$VT$$

```
> ID;
```

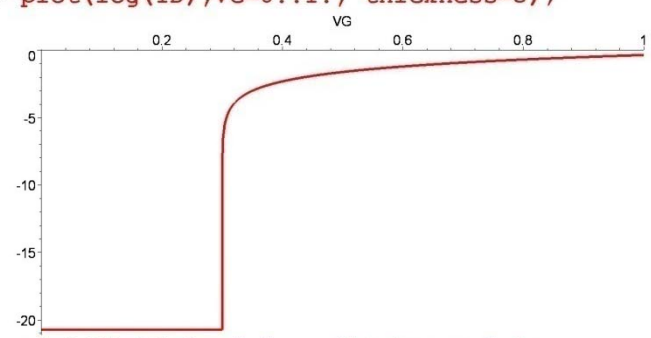
$$\begin{cases} ILeak & VG < VT \\ K\,(VG - VT) + ILeak & VT \le VG \end{cases}$$

```
>   K:=1: VT:=.3:  vth:=0.0259:  ILeak:=1E-9:
>
>
>
```

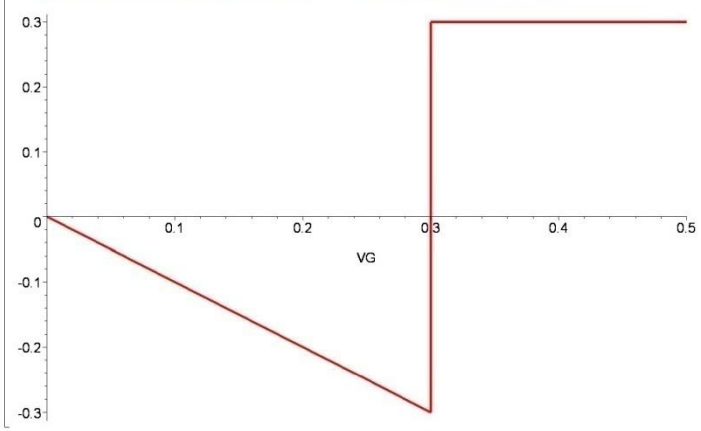
```
> plot((ID),VG=0..1., thickness=5);
```




```
> plot(log(ID),VG=0..1., thickness=5);
```




```
> plot(G1,VG=0..0.5,   thickness=5 );
```



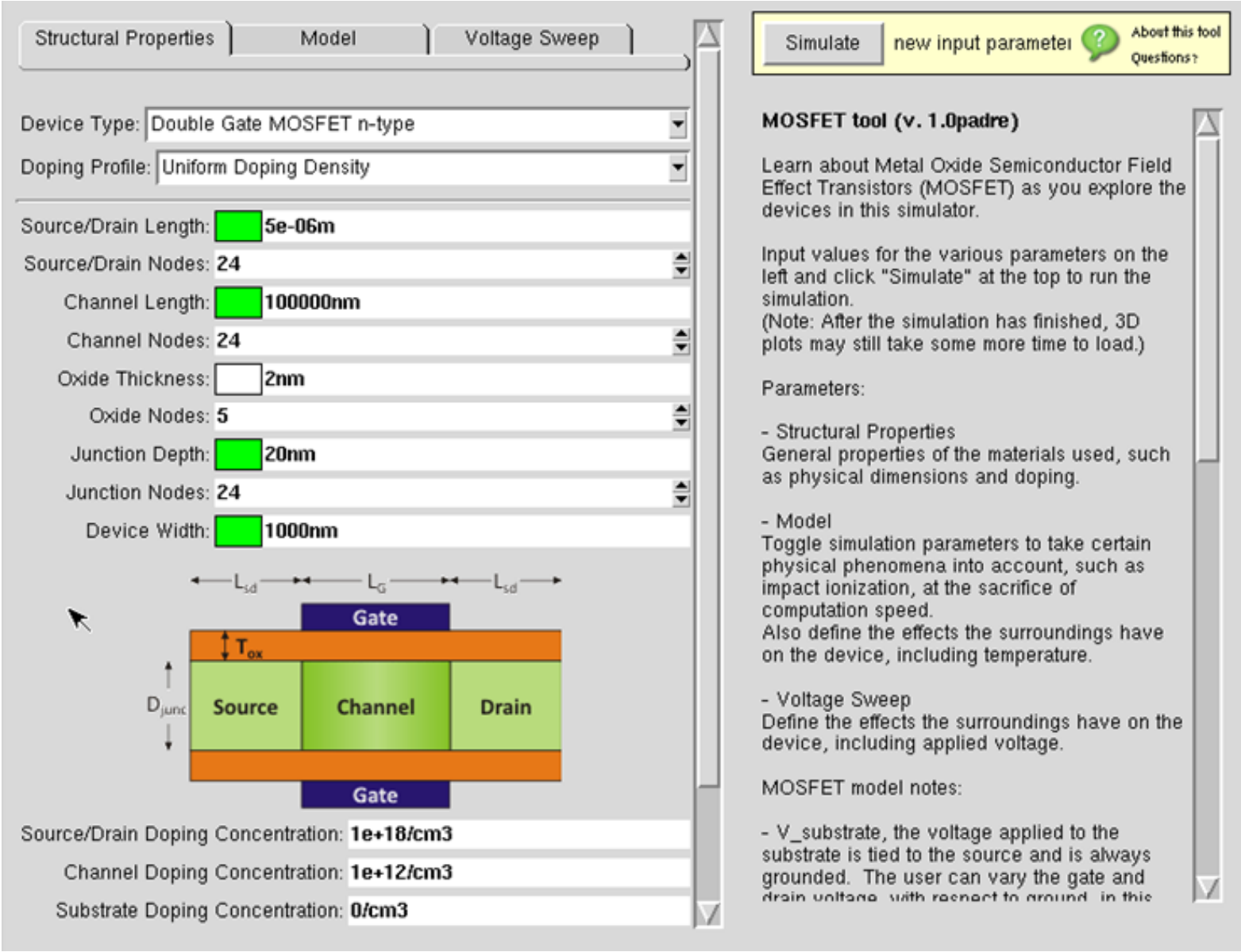
Derivatives of semi empirical approximation for I_D with Maple

```
> restart: with(plots): Digits:=20:  alias (W=LambertW):
Fit lateral Lambertiano de ID con degradation de movilidad-v6666.mws  21-jul-2012
> ID := (Io/(1+teta*VG))*W( (K1*(1+teta*VG))*exp( VG*b/n  )):
> der1:=diff(ID, VG):   der2:=diff(der1, VG):  der3:=diff(der2, VG):
> der1ln:=diff( ln(ID), VG):   der2ln:=diff(der1ln, VG):  der3ln:=diff(der2ln, VG):
Caso numerico ya que no hay solucion analitica
> vth:=0.0259:  b:=1/vth:  n:=1.5223 : Io:= 6.6648e-6: K1:=9.4081e-7:  teta:=
0.3528:
> VT:=fsolve ( der3, VG=0.4..0.6):   VTln:=fsolve ( der3ln, VG=0.4..0.6):
> IVT:=eval( ID, VG=VT):   IVTln:=eval( ID, VG=VTln):
> plot( {der1/1E-4}, VG=0.0..1.1):
> plot( {der2/5e-4}, VG=0.0..1.1):
> plot( {der3/4.5e-3}, VG=0.0..1.1):
> plot( {der1/1E-4,der2/5e-4,der3/4.5e-3}, VG=0.0..1.1):
> dvg:=0.01:     nmax:=110:
> for i from 0 by 1 to nmax do  vg[i]:=+0.0+i*dvg: id[i]:=eval(ID, VG=vg[i]):
deri1[i]:=eval(der1, VG=vg[i]):  deri2[i]:=eval(der2, VG=vg[i]):
deri3[i]:=eval(der3, VG=vg[i]): deri2ln[i]:=eval(der2ln, VG=vg[i]): end do:
> for i from 0 by 1 to nmax do  lprint(vg[i],id[i],deri1[i],deri2[i],deri3[i]) end do:
```

Verification with Maple of Karlsson & Jeppson method. ICMTS 2013.

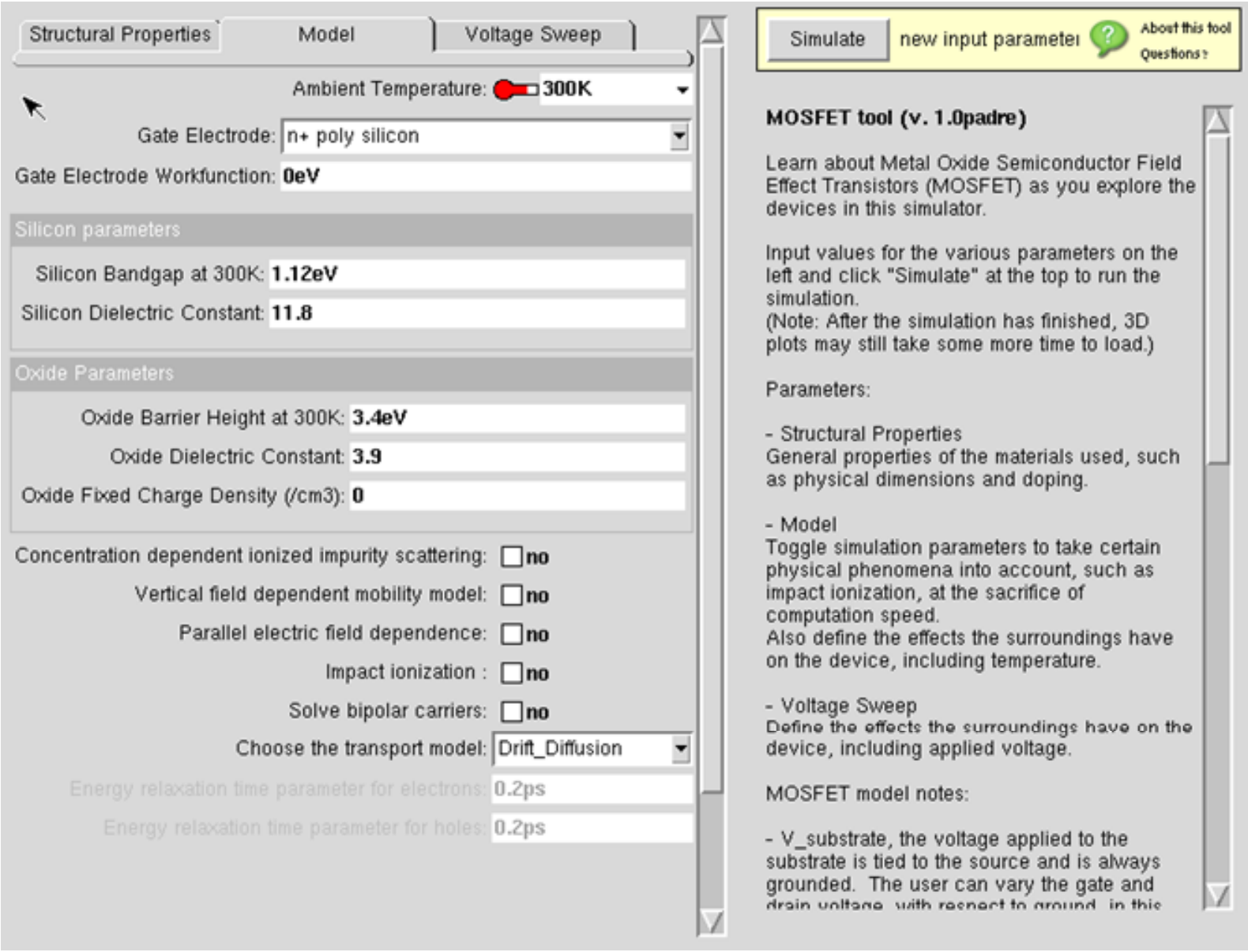
```
>> restart:
> ID:=K*(VG-VT-(VD/2) )*VD/(1+teta1*(VG-VT)+teta2*(VG-VT)**2):  ID1:=(a+b*VG)/(1+c*VG+d*VG**2 ):
> a:=-b*(VT+VD/2):     b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2):    d:=teta2/(1-teta1*VT+teta2*VT**2):
➢simplify(ID-ID1):
➢> restart;
> eq1:= a+b*(VT+VD/2):   eq2:= -b+K*VD/(1-teta1*VT+teta2*VT**2):
> eq3:= -c+(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2): eq4:= -d+teta2/(1-teta1*VT+teta2*VT**2):
> solve( {eq1,eq2,eq3,eq4}, {K,VT,teta1,teta2}):
>  restart;
> K1 := 4*b^3/(4*d*a*b*VD-4*c*b*a-2*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2)/VD:
> K2:=b/((1+c*VT+d*VT**2)*VD):
> a:=-b*(VT+VD/2):     b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2):    d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify(K1-K2):
> restart;
> teta1a := -4*(d*b*VD-c*b+2*d*a)*b/(4*d*a*b*VD-4*c*b*a-2*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2):
> teta1b := ( c+2*d*VT)/(1+c*VT+d*VT**2):
> a:=-b*(VT+VD/2):     b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2):    d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify( teta1a-teta1b):
> restart;
> teta2a := 4*d*b^2/(4*d*a*b*VD-4*c*b*a-2*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2):
> teta2b := d/(1+c*VT+d*VT**2):
> a:=-b*(VT+VD/2):     b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2):    d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify( teta2a-teta2b):
```

Using the “MOSFet” tool in nanohub: Structural Properties



“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.

Using the “MOSFet” tool in nanohub: Model



Using the “MOSFet” tool in nanohub: Voltage Sweep