Design of Digital Systems with FPGA

Objectives:

- Trainees will gain an understanding of the basic of the VHDL description for digital systems.
- Trainees will able to develop combinational systems, sequential systems or combinations of them.
- Trainees will develop the test bench for detecting and correcting errors before to implementation on FPGA.

Day 1 - Introduction

1. What is an FPGA?
2. VHDL
    a. Structure
    b. Identifiers
    c. Architecture
    d. Styles of design
3. Integrated Design Environment (IDE)
4. Practice 1

Day 2 – Basic Description

1. IEEE Std. Logic 1164
    a. Usage
    b. Compatibility
2. Logic gates
    a. AND
    b. OR
    c. XOR
    d. NOT
3. Signal types
4. Declarations
5. Practice 2

Day 3 – Combinational Logic

1. True tables
2. Karnaugh map
3. Multiplexers
4. IEEE Numeric Std.
    a. Usage
    b. Compatibility
5. Look-Up Tables (LUT)
    a. Definition
    b. Usage
6. Practice 3

Day 4 – Sequential Logic

1. Memory elements
2. Registers
3. Counters
4. State Machines
5. Practice 4

Notes:

1. The practices could be more than one per day.
2. Test Bench will be included before, during or after the practices.
3. Basics of digital systems is needed.
4. Program subject to minor changes.

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