High-K Dielectrics / High-Mobility Channel MOSFETs

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September 21, 2012

Puebla 's IEEE CAS and EDS Chapters

National Institute for Astrophysics, Optics and Electronics

High-K dielectrics such as HfO_2, ZrO_2 and HfSiON have attracted a great deal of attention for reduced power dissipation in CMOS applications. However, channel mobility degradation, charge trapping and reliability are major concerns. In this paper, we will review recent research results, e.g. the charge trapping characteristics, the effects of nitrogen on channel mobility. More recently high channel materials such as III-V, Ge and graphene with high-K dielectrics are attractive for achieving enhanced device performance for MOSFETs (Fig.1). To achieve high performance III-V n-MOSFETs, we have systematically investigated the effect of process annealing sequence, channel thickness/doping concentration and high-K gate stacks on device performance of surface channel InGaAs MOSFETs. High performance $In_{0.53}Ga_{0.47}As$ MOSFETs with optimized device structure and process will be presented. To further improve the channel mobility, we have also studied buried channel InGaAs MOSFETs with InP or InP/InAlAs barrier layers. We will also present our work on substrate structure optimization and mobility scattering mechanism on buried channel III-V MOSFETs. Highest channel mobility of ~5000 cm^2/Vs has been achieved by using $In_{0.7}Ga_{0.3}As$ channel with InP/InAlAs double-barrier and ALD Al_2O_3 oxide. Band gap engineering and gate stack scaling were applied to $In_{0.7}Ga_{0.3}As$ vertical tunneling FET (TFETs) with lower SS (86mV/dec) and higher I_d (50μA/μm) vs. previously reported data (Fig. 2).

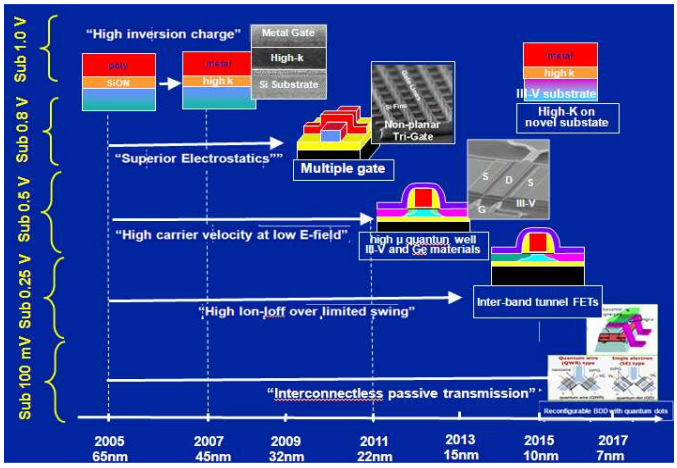

Fig. 1: High-mobility channel (e.g. III-V materials) MOSFETs and tunnel FETs are to be incorporated into CMOS in the near future [Source: Intel].

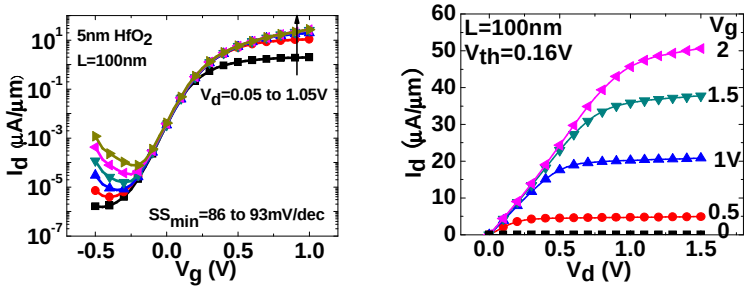

Fig. 2: The smallest subthreshold swing of 86 mV/dec and I_{on} of 50 mA/mm at V_g=2 V was achieved by TFETs with 5 nm HfO_2 (EOT=1.2 nm). The gate leakage current is less than 1×10^{-4} A/cm^2 at V_g=1 V.