Exploring MOSFET threshold voltage extraction methods

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Distinguished Lecture Program
1. Introduction:
The threshold voltage is a fundamental parameter for reliability assessment.
Our 2002 review article [OR02] has 133 citations in Scopus (see tables from 26/Aug/2013).
Since then there have been many additional publications about threshold voltage extraction methods.
We have just updated our review paper [OR13].
Both review articles have been in the list of the top 25 hottest articles in Microelectronics and Reliability.
We are now updating both papers.


"Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
Our previous article [OR02] reviewed 14 methods to extract $V_T$

For crystalline MOSFETs biased in the linear region:
1) Constant-current (CC)
2) Linear extrapolation (LE)
3) Transconductance Linear extrapolation (GMLE) from Tsuno in 1998.
4) Second Derivative (SD) from Wong in 1987.
5) Current-to-square-root-Transconductance Ratio ($\text{CsrTR} = I_D / gm^{0.5}$) by independent work by Jain and and by Ghibaudo in 1988.
6) Transition (based on integration) and it was developed by us in 2000.
7) Integral (based on integration) and it was developed by us in 1997.
8) Corsi (based on an auxiliary function) published in 1993.
9) Second Derivative logarithmic (SDL) proposed by Aoyama in 1995.
10) Linear cofactor difference operator (LCDO) developed by He in 2002.
11) Non-linear optimization

For crystalline MOSFETs biased in the saturation region:
1) Linear extrapolation (LE)
2) $G_1$ function developed by us in 2001

For non-crystalline MOSFETs biased in the saturation region:
1) H function developed by us in 2001


"Exploring MOSFET threshold voltage..." EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
Boudinet reviewed [BO09] eight $V_T$ extraction methods

1) Linear extrapolation (LE)
2) Transconductance Linear extrapolation (GMLE) from Tsuno in 1998.
3) Second Derivative (SD) from Wong in 1987.
4) Current-to-square-root-of-Transconductance Ratio (CsrTR $=I_D/g_m^{0.5}$) by independent work by Jain and and by Ghibaudo in 1988.
5) Corsi (based on an auxiliary function) published in 1993.
6) Second Derivative logarithmic (SDL) proposed by Aoyama in 1995.
7) Linear cofactor difference operator (LCDO) developed by He in 2002.
8) Transition (based on integration) and it was developed by García Sánchez et al in 2000.

They recommended: SD, CsrTR, and LCDO methods.

To compare the different methods, we will apply them to measured characteristics [HO12,OR13] of a state-of-the art MOSFET with:

- \( W = 5 \, \mu \text{m} \)
- \( L = 65 \, \text{nm} \)
- \( t_{ox} = 2.6 \, \text{nm} \)


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2.1. Constant-Current (CC) method

Threshold voltage is defined as the value of gate voltage corresponding to a given (arbitrary) constant drain current.Tsuno proposed [TS99] that this constant drain current be $(W_m/L_m) \times 10^{-7}$ where $W_m$ and $L_m$ are the mask channel width and length, respectively.

Bazigos recently proposed [BA11] that this constant drain current should be dependent on drain voltage in order to obtain a consistent threshold voltage in the saturation region.


Semi-empirical approximation for small $V_D$ [OR13]:

\[
I_D = \frac{I_o}{(1 + \theta V_{GS})} W \left[ K \left(1 + \theta V_{GS}\right) e^{\frac{V_{GS}}{n v_{th}}} \right] \quad \Rightarrow \quad V_{GS} = \frac{n v_{th} \ln (I_D) + \left(\frac{n v_{th}}{I_o}\right) I_D - n v_{th} \ln (K I_o)}{1 - \left(\frac{n v_{th}}{I_o}\right) I_D}
\]
2.2. Match-Point (MP) method

The MP method [KA90] establishes that $V_T$ occurs at the gate voltage for which the exponential extrapolation of subthreshold current deviates by 5% from the measured current.

It overemphasizes weak inversion and neglects strong inversion.


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2.3. Linear Extrapolation (LE) method

For the linear region: It consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the $I_D-V_G$ curve linear extrapolation at its maximum first derivative point.

Then, the value of $V_T$ is often calculated by subtracting $V_D/2$ from the resulting gate-voltage axis intercept.

For the saturation region: The LE method, is similar to that in the linear region but it uses the $I_{Dsat}^{0.5}-V_G$ characteristics instead.
Linear Extrapolation (LE) method

- Measured data
- Linear extrapolation

$V_T = 0.57 \text{ V}$

$V_D = 10 \text{ mV}$

Maximun slope at $V_G = 0.79 \text{ V}$

$V_D = 1.1 \text{ V}$

Linear Extrapolation (LE) method in saturation

- Measured data
- Linear extrapolation

$V_T = 0.41 \text{ V}$
2.4. Second-derivative (SD) method

It determines $V_T$ as the gate voltage at which the second derivative of the current (i.e., $d^2I_D/dV_G^2$) is maximum [WO87].

The origin of this method can be understood by analyzing Level=1 SPICE model, where $I_D=0$ for $V_G < V_T$ and $I_D$ is proportional to $V_G$ for $V_G > V_T$.

Using above assumption, $dI_D/dV_G$ becomes a step function, and $d^2I_D/dV_G^2$ is a Dirac delta function.

For a real device $d^2I_D/dV_G^2$ will exhibit a maximum at $V_G = V_T$.

Measurement noise can be reduced by numerical smoothing techniques, or by fitting the semi empirical model described previously to the measured data, and thereafter performing the numerical derivatives.

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Andrade and Martino [AN08], using the SD method, observe various $V_T$ for SOI MuGFETs.

For DG transistors, one or two $V_T$ can be observed [AN08], depending on the channel doping concentration.

For triple-gate and quadruple-gate it is possible to observe up to four $V_T$ due to corner effects and different doping concentration between the top and bottom of the Fin.

2.5. Third-derivative (TD) method

The TD method [WO01] determines \( V_T \) as the gate voltage at which the third derivative of the current (i.e., \( d^3 I_D/dV_G^3 \)) is maximum.

The maximum and minimum of \( d^3 I_D/dV_G^3 \) are always located to the left and right of the maximum of \( d^2 I_D/dV_G^2 \), as is illustrated in the figure.

Therefore, this method is inconsistent with the second derivative method.


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The Third-derivative (TD) method suffers from severe problems from experimental noisy data. The measurement noise can be reduced with numerical smoothing techniques or by fitting the semi empirical model described previously to the measured data, and thereafter performing the numerical derivatives.
2.6. Current-to-square-root-Transconductance Ratio ($C_{srTR}$) method

For strong inversion [JA88; GH88; FI95; SU10;JO11] :

$$C_{srTR} \equiv \frac{I_D}{\sqrt{g_m}} \equiv \frac{I_D}{\sqrt{dI_D/dV_G}} = S^{-1/2} \left( V_G - V_T \right)$$

For weak to strong inversion, the empirical model yields:

$$C_{srTR} \equiv \frac{I_D}{g_m^{1/2}} = \sqrt{n \nu_{th} I_o W \left( K e^{\beta V_G} \right)} \left[ 1 + W \left( K e^{\beta V_G} \right) \right]$$

$$V_G = n \nu_{th} \left[ \ln \left( -1 + \sqrt{1 + \frac{4 C_{srTR}^2}{n \nu_{th} I_o}} \right) + \frac{1}{2} \sqrt{1 + \frac{4 C_{srTR}^2}{n \nu_{th} I_o}} - \frac{1}{2} - \ln(2 K) \right]$$


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Current-to-square-root-of-Transconductance Ratio (CsrTR) method

- measured data
- linear extrapolation: $V_T=0.61 \text{ V}$
- fitted model: $V_T=0.55 \text{ V}$

Current-to-square-root-of-Transconductance Ratio (CsrTR) method in saturation

- measured data
- extrapolation: $V_T=0.46 \text{ V}$

$$C_{srTR} \equiv \frac{I_D}{\sqrt{dI_D/dV_G}}$$

$$C_{srTR_{sat}} \equiv \frac{\sqrt{I_D}}{\sqrt{d\sqrt{I_D}/dV_G}}$$

"Exploring MOSFET threshold voltage..." EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
Tsormpatzoglou et al [TS12] recently proposed an improvement of the current-to-square-root-Transconductance Ratio (CsrTR) method.

A simplified variation of this method will now be described. The following equation is valid for weak to strong inversion:

\[
V_g = V_T + V_{th} \ln \left( e^{\left( \frac{4 \text{CsrTR}^2}{B^2 + \sqrt{B^4 + 4B^2 \text{CsrTR}^2}} \right)} \left( \frac{B^2 - \sqrt{B^4 + 4B^2 \text{CsrTR}^2}}{4B^4} \right)^2 \right)
\]

where \( B \equiv 2V_{th} \sqrt{\beta V_d} \)

In order to extract \( V_T \) and \( \beta \), and avoid second order effects, the previous equation is fitted for values close to \( V_T \).


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The range of $V_G$, for extracting $V_T$ and $\beta$, is estimated by the linear fit method.

The model presents serious errors for weak inversion.

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Comparison of the equation proposed by Tsormpatzoglou and our empirical model

The equation proposed by Tsormpatzoglou is simplified to:

\[ V_G = V_T - 2\ln(2)\nu_{th} + 2\nu_{th}\ln\left(\sqrt{1 + 4\left(\frac{CsrTR}{B}\right)^2} - 1\right) + \frac{4\nu_{th}\left(\frac{CsrTR}{B}\right)^2}{\sqrt{1 + 4\left(\frac{CsrTR}{B}\right)^2} + 1} \]

Our empirical model is:

\[ V_G = V_T - n\nu_{th}\ln(2K) + n\nu_{th}\ln\left(-1 + \sqrt{1 + \frac{4CsrTR^2}{n\nu_{th}I_o}}\right) + \frac{n\nu_{th}}{2}\left(\sqrt{1 + \frac{4CsrTR^2}{n\nu_{th}I_o}} - 1\right) \]

The models are different although they present some similarities.

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Jeon et al recently applied [JE13] the current-to-square-root-Transconductance Ratio (CsrTR) method to junctionless transistors. The CsrTR method could yield to two slopes. The SD method could also yield to two $V_T$. For $V_G \ll V_{FB}$ the device is in full depletion. When $V_G = V_{FB}$, the device becomes neutral. For $V_G \gg V_{FB}$, the device is in accumulation. Therefore, there are two successive conduction regimes separated by $V_{FB}$: volume and accumulation conduction.


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Ortega and coworkers from INAOE [OR10] also used the current-to-square-root-Transconductance Ratio (CsrTR) method.

\[ CsrTR = \sqrt{k_o V_D (V_G - V_T)} \]

\( V_T \), the effective channel, the series resistance and the mobility degradation are extracted.


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Emrani et al [EM93] generalized the CsrTR method to account for other mobility models at low temperature.

Assuming a mobility model such as

\[ I_D = K \frac{(V_G - V_T)^{n-1}}{(1 + \theta^{n-1}(V_G - V_T)^{n-1})} \]

It can be proved:

\[ C_{srTR} \propto (V_G - V_T)^{2/n} \]

For \( n=3 \):

\[ I_D = K \frac{(V_G - V_T)^2}{(1 + \theta^2(V_G - V_T)^2)} \]

\[ C_{srTR} \propto (V_G - V_T)^{2/3} \]


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The previous generalization has been recently used [CH12;13] for nanocrystalline ZnO thin film transistors

They used $n=3$:

$$I_D = K \frac{(V_G - V_T)^2}{\left(1 + \theta^2 (V_G - V_T)^2\right)}$$

$$CsrTR \propto \left( V_G - V_T \right)^{2/3}$$


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2.7. Transition method
This method [GA00] was inspired on the integral difference function $D$, which was defined for a two-terminal device as [GA95,96]:

$$D(V,I) \equiv \int_0^I V dI - \int_0^V I dV = VI - 2 \int_0^V I dV$$

This function has the property of eliminating the effect of any resistance connected in series with the device. The transition method proposes to use the function $G_1$:

$$G_1(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D} = \left(V_G - V_{Gi}\right) - 2 \int_{V_{Gi}}^{V_G} \frac{I_D}{I_D} dV_G$$


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The origin of the transition method can be understood by analyzing the ideal case of a MOSFET: \( I_D = I_{\text{leak}} \) for \( V_G < V_T \) and \( I_D \propto V_G \) for \( V_G > V_T \).

Using these assumptions, we observe that:
(a) \( G_1 \) has a discontinuity at \( V_T \);
(b) \( G_1 = -V_G \) for \( V_G < V_T \); and
(c) \( G_1 = +V_T \) for \( V_G > V_T \).

For a real device function \( G_1 \) will have a maximum due to the mobility degradation and its value will be close to \( V_T \).

\[
G_1 = V_G - 2 \int_{0}^{V_G} I_D \, dV_G
\]
\[ G_1(V_G, I_D) = \frac{D(V_G, I_D)}{I_D} = (V_G - V_{G_i}) - 2 \left( \frac{V_G}{I_D} \right) \]

\[ G_{1sat}(V_G, I_D) = (V_G - V_{G_i}) - 2 \left( \frac{V_G}{\sqrt{I_D}} \right) \]

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2.8. Normalized Mutual Integral Difference (NMID) Method

This method [HE02] is inspired in normalizing the function $D$:

$$D_{\text{normal}}(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D V_G} = 1 - 2 \int_{0}^{V_G} \frac{I_D}{I_D V_G} dV_G$$

Accordingly, a plot of $D_{\text{normal}}$ versus $V_G$ will have a maximum at the value of $V_T$.

Notice that the location of a maximum is independent of the constant and thus, the term “-1” can be removed.

A disadvantage of this method is that the maximum is located in a broad region.

In the next section we will present an improvement of the present method.


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\[ D_{\text{normal}}(V_G, I_D) = \frac{D(V_G, I_D)}{I_D V_G} = 1 - 2 \int_0^{V_G} \frac{I_D}{I_D V_G} dV_G \]

\[ D_{\text{normal-sat}}(V_G, \sqrt{I_D}) = 1 - 2 \int_0^{V_G} \frac{\sqrt{I_D}}{\sqrt{I_D V_G}} dV_G \]

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2.9. Normalized Reciprocal H (NRH) function method

By removing the -1 term and the factor 2 from the previous method and considering that the current is not zero at $V_G = 0$, we can obtain a normalized version of our previous $H$ function which was originally proposed in 2001 [OR01] for extracting the threshold voltage of amorphous thin film MOSFETs, and it was revised in 2010 [OR10] to evaluate the sub-threshold slope of MOSFETs:

$$H_{normal}(V_G) = \frac{\int_0^{V_G} I_D(V_G) \, dV_G}{V_G \left[ I_D - I_D(V_G = 0) \right]}$$


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In order to obtain results with maximum or minimum in narrow regions, we propose to use the reciprocal of the previous function:

\[
H_{nr}(V_G) = \frac{V_G \left[ I_D - I_{D_0}(V_G = 0) \right]}{2 \int_0^{V_G} I_D(V_G) \, dV_G}
\]

A factor of 2 was included in order to obtain the following simple graphical interpretation:

1. The numerator divided by 2 is the area of a triangle with a width of \( V_G \) and a height of \( I_D - I_{D_0}(V_G = 0) \).

2. Then, \( H_{nr} \) is the ratio of the area of this triangle divided by the area under the plot (the integration).
Normalized reciprocal $H$ (NRH) function method

$$H_{nr} \left( V_G \right) = \frac{V_G \left[ I_D - I_D \left( V_G = 0 \right) \right]}{\int_{0}^{V_G} I_D \left( V_G \right) dV_G}$$

Normalized reciprocal $H$ (NRH) function method in saturation

$$H_{nr-sat} \left( V_G \right) = \frac{V_G \left[ \sqrt{I_D} - \sqrt{I_D \left( V_G = 0 \right)} \right]}{\int_{0}^{V_G} \sqrt{I_D} dV_G}$$

$V_D = 10 \text{ mV}$  $V_T = 0.46 \text{ V}$

$V_D = 1.1 \text{ V}$  $V_T = 0.47 \text{ V}$

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2.10. Transconductance-to-Current-Ratio (TCR) methods

The function $g_m/I_D$ has been used for device characterization for more than 3 decades [TS82]:

$$TCR = \frac{g_m}{I_D} = \frac{1}{I_D} \frac{dI_D}{dV_G} = \frac{d \ln(I_D)}{dV_G}$$

2.10.1 SDL by Aoyama in 1995 [AO95]

The TCR methods can be related to the pioneering publication by Aoyama in 1995 [AO95], who proposed that $V_T$ be determined as the gate voltage at which the Second Derivative of the Logarithm (SDL) of the drain current takes on a minimum value:

$$V_T \equiv V_G \text{ at } \left. \frac{d^2 \ln(I_D)}{dV_G^2} \right|_{\text{min}}$$

Measurement noise is significant. Aoyama was using TCR without probably knowing it.


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2.10.2 TCR by Cunha et al in 2005 [CU05;GA07]

They proposed [CU05;GA07] that $V_T$ be determined as the value of $V_G$ at which TCR is equal to half of its maximum value.

$$V_T \equiv V_G \text{ at } \frac{TCR_{max}}{2}$$

This definition has been related [CU11,SI12] to the condition that diffusion and drift current be equal.


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Doria et al [DO13] recently applied the TCR method to junctionless transistors.

The previous definition of $V_T$ ($V_G$ at which TCR is equal to half of its maximum value) was recently used [DO13] for junctionless nanowire transistors.

Numerical simulations [DO13] show that this definition coincides with the condition that diffusion and drift current be equal.

![Graph](image)

Fig. 3 in [DO13] “Drift and diffusion components of the current (left axis) and the transconductance to the current ratio (right axis) as a function of the gate voltage for two temperatures”.


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2.10.3 TCR by Flandre and his group in 2010 [FL10]

They proposed [FL10] that $V_T$ be defined at the location of the maximum slope of TCR. Using:

$$\frac{d^2 \ln(I_D)}{dV_G^2} = \frac{d\ TCR}{dV_G}$$

$$V_T \equiv V_G \text{ at } \frac{d\ TCR}{dV_G} \bigg|_{\text{max}}$$

$$\equiv V_G \text{ at } \frac{d\ TCR}{dV_G} \bigg|_{\text{min}} = V_G \text{ at } \frac{d^2 \ln(I_D)}{dV_G^2} \bigg|_{\text{min}}$$

Therefore, this definition is mathematically equivalent to SDL. It has been related to the threshold voltage obtained from C-V.

Measurement noise is significant.


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2.10.4 TCR by Rudenko et al in 2011 [RU11a,b]

In order to reduce the noise effects due to the derivative, they proposed [RU11a,b] to define the threshold voltage as the gate bias at which TCR is 2/3 of its maximum value.

\[ V_T \equiv V_G \text{ at } \frac{2 TCR_{\text{max}}}{3} \]

Measurement noise is not significant.


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2.11. Reciprocal H (RH) methods

$\text{TCR} (= g_m / I_D)$ is equivalent to the inverse of the sub-threshold slope factor:

$$S = \frac{\ln(10)}{d \ln(I_D)} = \frac{I_D}{g_m} \ln(10)$$

$$d \frac{V_G}{V_G}$$

Considering that $\text{TCR}$ significantly increases measurement noise, especially in weak inversion, an equivalent function for low gate bias, based on integrations was proposed in 2010 [OR10] :

$$H_r(V_G) = \left[ \frac{I_D - I_D(V_G = 0)}{V_G} \right]$$

$$\int_{0}^{V_G} I_D(V_G) dV_G$$

The RH method [OR13] proposes that $V_T$ be defined by the maximum slope of function $H_r$.


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Transconductance-to-Current-Ratio (TCR) and Reciprocal H function (RH)
methods in saturation

a) defined at 2/3 of the maximum value: $V_{Tsat} = 0.45 \text{ V}$

b) defined at the maximum slope

From $TCR_{sat}$: $V_{Tsat} = 0.44 \text{ V}$

From $RH_{sat}$: $V_{Tsat} = 0.52 \text{ V}$

\[
TCR = \frac{d \ln(I_D)}{dV_G}
\]

\[
H_r(V_G) = \left[ I_D - I_D(V_G=0) \right] \int_0^{V_G} I_D(V_G) \, dV_G
\]

\[
H_{r-sat}(V_G) = \left[ \sqrt{I_D} - \sqrt{I_D(V_G=0)} \right] \int_0^{V_G} \sqrt{I_D} \, dV_G
\]

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It requires at least two output characteristics.


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This method is based on:

\[ I_D = \frac{W \mu_C}{L(1+\theta V_G)} \left(V_G - V_G - \frac{V_D}{2}\right) V_D \]

First, we measure \( G \). Then, we fit the following straight line to obtain \( A \) and \( B \):

\[ G = \frac{d I_D}{d V_D} = A - B V_D \]

<table>
<thead>
<tr>
<th>( V_G ) (V)</th>
<th>( A ) (mA/V)</th>
<th>( B ) (mA/V²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{G1} = 0.75 )</td>
<td>2.08</td>
<td>10.8</td>
</tr>
<tr>
<td>( V_{G2} = 1 )</td>
<td>4.94</td>
<td>14.9</td>
</tr>
</tbody>
</table>

Evaluating:

\[ \eta_a = \frac{A}{A} \bigg|_{V_G = V_{G1}} = \frac{2.08}{4.94} = 0.42 \]

\[ \eta_b = \frac{B}{B} \bigg|_{V_G = V_{G1}} = \frac{10.8}{14.9} = 0.72 \]

\[ V_T = \frac{\eta_b V_{G1} - \eta_a V_{G2}}{\eta_b - \eta_a} = 0.40 \text{V} \]

This method yield to a low value of \( V_T \).

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2.13 Nonlinear optimization methods

2.13.1 The three-point direct extraction by Hamer [HA86]

\[ I_D = K \left( \frac{V_G - V_T - \frac{V_D}{2}}{1 + \theta \left( V_G - V_T \right)} \right) V_D \]

can be transformed into

\[ I_D = \frac{a + bV_G}{1 + cV_G} \]

where

\[ a = -b \left( V_T + \frac{V_D}{2} \right) \]

\[ b = \frac{KV_D}{1 - \theta V_T} \]

\[ c = \frac{\theta}{1 - \theta V_T} \]

The parameters a, b, and c can be determined from three measurements or by fitting it to the complete data. Knowing a, b and c, the device parameters are evaluated by:

\[ K = \frac{b}{(1 + c V_T)V_D} \]

\[ V_T = -\frac{a}{b} - \frac{V_D}{2} \]

\[ \theta = \frac{c}{1 + c V_T} \]


“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
2.13.2 The four-point direct extraction by Karlsson and Jeppson [KA93;JE13]

\[ I_D = K \frac{V_G - V_T - \frac{V_D}{2}}{1 + \theta_1 \left( V_G - V_T \right) + \theta_2 \left( V_G - V_T \right)^2} V_D \]

is transformed into

\[ I_D = \frac{a + b V_G}{1 + c V_G + d V_G^2} \]

where \[ a = -b \left( V_T + \frac{V_D}{2} \right) \]

\[ b = \frac{K V_D}{1 - \theta_1 V_T + \theta_2 V_T^2} \]

\[ c = \frac{\theta_1 - \theta_2 V_T}{1 - \theta_1 V_T + \theta_2 V_T^2} \]

\[ d = \frac{\theta_2}{1 - \theta_1 V_T + \theta_2 V_T^2} \]

The parameters \( a, b, c \) and \( d \) can be determined from three measurements or by fitting it to the complete data. Knowing \( a, b, c \) and \( d \), the device parameters are evaluated by:

\[ K = \frac{b}{\left(1 + c V_T + d V_T^2\right) V_D} \]

\[ V_T = -\frac{a}{b} - \frac{V_D}{2} \]

\[ \theta_1 = \frac{c + 2d V_T}{1 + c V_T + d V_T^2} \]

\[ \theta_2 = \frac{d}{1 + c V_T + d V_T^2} \]

By setting \( \theta_1 = \theta \) and \( \theta_2 = 0 \) (d=0), this method yield to the previous three-point method.


“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
The obtained fitting parameters are:

<table>
<thead>
<tr>
<th>Number of Parameters</th>
<th>a (µA)</th>
<th>b (µA/V)</th>
<th>c (V⁻¹)</th>
<th>d (V²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>-65.31</td>
<td>117.23</td>
<td>5.3e-5</td>
<td>0.1053</td>
</tr>
<tr>
<td>3</td>
<td>-71.22</td>
<td>127.83</td>
<td>0.2055</td>
<td></td>
</tr>
</tbody>
</table>

Then, the extracted parameters are:

<table>
<thead>
<tr>
<th>Number of Parameters</th>
<th>V₇ (V)</th>
<th>K (mA/V²)</th>
<th>θ₁ (V⁻¹)</th>
<th>θ₂ (V²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.5521</td>
<td>11.4</td>
<td>0.1127</td>
<td>0.1020</td>
</tr>
<tr>
<td>3</td>
<td>0.5522</td>
<td>11.5</td>
<td>0.1845</td>
<td></td>
</tr>
</tbody>
</table>

For this particular case, both models (3 and 4 parameters) yields approximately to the same reasonable results.

These methods require non-linear optimization.
Comparison of various threshold voltage methods  

<table>
<thead>
<tr>
<th>Method</th>
<th>( V_T ) (V) in linear region ((V_D = 10 \text{ mV}))</th>
<th>( V_T ) (V) in saturation region ((V_D = 1.1 \text{ V}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant Current (CC)</td>
<td>0.57</td>
<td>0.45</td>
</tr>
<tr>
<td>Match-Point (MP)</td>
<td>0.35</td>
<td>0.31</td>
</tr>
<tr>
<td>Linear Extrapolation (LE)</td>
<td>0.57</td>
<td>0.41</td>
</tr>
<tr>
<td>Second Derivative (SD)</td>
<td>0.55</td>
<td>0.45</td>
</tr>
<tr>
<td>Third-derivative (TD)</td>
<td>0.48</td>
<td>NA*</td>
</tr>
<tr>
<td>Current-to-square-root-Transconductance Ratio (CsrTR)</td>
<td>0.61</td>
<td>0.46</td>
</tr>
<tr>
<td>Linear by Jain and Ghibaudo (1988)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current-to-square-root-Transconductance Ratio (CsrTR) by us using empirical model (2013)</td>
<td>0.55</td>
<td>NA*</td>
</tr>
<tr>
<td>Current-to-square-root-Transconductance Ratio (CsrTR) by Tsormpatzoglou (2012)</td>
<td>0.59</td>
<td>NA*</td>
</tr>
</tbody>
</table>

“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.

*NA means Not Applicable
Comparison of various threshold voltage methods  2/2

<table>
<thead>
<tr>
<th>Method</th>
<th>( V_T ) (V) in linear region ((V_D = 10 \text{ mV}))</th>
<th>( V_T ) (V) in saturation region ((V_D = 1.1 \text{ V}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition</td>
<td>0.54</td>
<td>0.37</td>
</tr>
<tr>
<td>Normalized Mutual Integral Difference (NMID)</td>
<td>0.46</td>
<td>0.47</td>
</tr>
<tr>
<td>Normalized Reciprocal H (NRH)</td>
<td>0.46</td>
<td>0.47</td>
</tr>
<tr>
<td>SDL by Aoyama (1995) or TCR at Maximum slope by Flandre (2010)</td>
<td>0.53</td>
<td>0.44</td>
</tr>
<tr>
<td>TCR at (1/2) TCR(_{\text{max}}) by Cunha (2005)</td>
<td>0.56</td>
<td>NA*</td>
</tr>
<tr>
<td>TCR at (2/3) TCR(_{\text{max}}) by Rudenko (2011)</td>
<td>0.49</td>
<td>NA*</td>
</tr>
<tr>
<td>Reciprocal H (RH)</td>
<td>0.55</td>
<td>0.52</td>
</tr>
<tr>
<td>Conductance method presented in a recent Chinese Patent</td>
<td>0.40</td>
<td>NA*</td>
</tr>
<tr>
<td>Nonlinear optimization methods</td>
<td>0.55</td>
<td>NA*</td>
</tr>
</tbody>
</table>

“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.

*NA means Not Applicable
3. 2-D simulations for several S/D regions length

Increasing S/D regions’ length is equivalent to increasing the series resistance.

Simulations of an undoped DG MOSFET ($V_{FB} = -1.03$V), using the “MOSFet” tool [MA12], were carried out with constant mobility and S/D regions length varying from 10 nm to 10 μm. Other used parameters were: $n^+$ polysilicon gate, S/D with doping concentrations of $10^{18}$ cm$^{-3}$, a body doping concentrations of $10^{12}$ cm$^{-3}$ and a 100-μm channel length.


“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
*V_T* versus S/D regions length

LE and Transition methods depend strongly on series resistance.

CsrTR, CC and NRH methods are weakly dependent on series resistance.

SD, SDL, NMID, RH, and CsrTR Lambert methods do not depend on series resistance.
Transfer characteristics 2-D simulations for different values of drain voltage

Simulations of $I_D(V_G)$ with several values of $V_D$ for an undoped DG MOSFET, using the “MOSFet” tool [MA12], were carried out with a S/D regions length of 5 μm.


"Exploring MOSFET threshold voltage..." EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
**$V_T$ versus $V_D$**

LE, CsrTR, and Transition methods depend strongly on drain voltage.

SD and CsrTR Lambert methods are weakly dependent on drain voltage.

SDL, NMID, CC (from Bazigos), NRH and RH methods do not dependent on drain voltage.

“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
4. $V_T$ extraction for non-crystalline MOSFETs

The weak inversion current ($I_{Dw}$) is modeled by:

$$I_{Dw} = I_0 \exp\left(\frac{V_G}{nV_{th}}\right)$$

where $I_0$ is a global coefficient and $n$ is the subthreshold ideality factor.

The strong inversion current ($I_{Ds}$), at low drain voltage, exhibit a monomial type equation:

$$I_{Ds} = K \left(V_G - V_{Ts}\right)^m V_D$$

where $K$ is a global conduction coefficient, $m$ is the monomial’s order, usually around 2, and $V_{Ts}$ is the $I_{Ds}=0$ intercept, which can be viewed as a “strong inversion region-defined” threshold voltage.

There are two recent review articles about integration-based parameter extraction methods: for MOSFET [OR08] and for two-terminal devices [GAO08].


“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
4.1. Single Integration method: $H_1$ function

An integration-based method was proposed in 2001 for extracting model parameters of non-crystalline MOSFETs biased in the saturation region [OR01]. The auxiliary function used in that method had been originally proposed in 1999 by our group to extract the model parameters of PN junctions at very low forward voltages [RA99].

The auxiliary function has the form:

$$H_1(I_D, V_G) = \frac{\int_{V_{Glow}}^{V_G} I_D(V_G) \, dV_G}{I_D - I_{low}}$$

where $I_{low} = I_D(V_G = V_{Glow})$, and $V_{Glow}$ is the lower limit of integration.


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For weak inversion:

$$I_{Dw} = I_o \exp\left(\frac{V_G}{nV_{th}}\right)$$

$$H_{1w}(V_G, I_D) \equiv \frac{\int_{V_G}^{V_{Glow}} I_D(V_G) \, dV_G}{I_D - I_{low}} = \frac{nV_{th}I_0}{I_0} \left[\exp\left(\frac{V_G}{nV_{th}}\right) - 1\right] = nV_{th}$$

which allows to extract $n$ from a constant value.

For strong inversion:

$$I_{Ds} = K \left(V_G - V_{Ts}\right)^m V_D$$

$$H_{1s}(V_G, I_D) \equiv \frac{\int_{V_G}^{V_{Glow}} I_D(V_G) \, dV_G}{I_D - I_{low}} = \frac{V_G - V_{Ts}}{m + 1}$$

which allows to extract $m$ and $V_{Ts}$ from an straight line.

The use of $H_1$ is an improvement over derivative-based methods regarding data noise reduction.

However, because $H_1$ still contains the possibly noisy raw current data in the denominator, it was proposed the use of a double integration method to further improve the noise immunity of the procedure.
4.2. Double Integration method: \( H_2 \) function

The previous idea was taken one step further with the purpose of reducing even more the effect of data noise. Function, \( H_2 \), based on successive double integration, was proposed [OR10b]:

\[
H_2(V_G, I_D) \equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) \, dV_G \, dV_G}{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} [I_D(V_G) - I_D(V_G = V_{Glow})] \, dV_G}
\]

\[
= \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) \, dV_G \, dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G) \, dV_G - I_{low} \, V_G}
\]

For weak inversion: \( I_{Dw} = I_o \exp \left( \frac{V_g}{n \nu_{th}} \right) \)

\[
H_{2w}(V_G, I_D) \equiv \frac{\int_{V_G}^V \int_{V_G}^V I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^V \int_{V_{Glow}}^V I_D(V_G) dV_G - I_{low} V_G} = n \nu_{th} \frac{n \nu_{th} \left[ \exp \left( \frac{V_G}{n \nu_{th}} \right) - 1 \right] - V_G}{n \nu_{th} I_{low} \left[ \exp \left( \frac{V_G}{n \nu_{th}} \right) - 1 \right] - I_{low} V_G} = n \nu_{th}
\]

which allows to extract \( n \) from a constant value.

For strong inversion: \( I_{Ds} = K \left( V_G - V_{Ts} \right)^m V_D \)

\[
H_{2s}(V_G, I_D) \equiv \frac{\int_{V_G}^V \int_{V_G}^V I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^V \int_{V_{Glow}}^V I_D(V_G) dV_G - I_{low} V_G} = \frac{V_G - V_{Ts}}{m + 2}
\]

which allows to extract \( m \) and \( V_{Ts} \) from an straight line.

The use of \( H_2 \) is an improvement with respect to \( H_1 \) regarding data noise reduction.
Both procedures were applied to a polycrystalline silicon nanowire n-channel MOSFETs, fabricated at the National Chiao Tung University, Hsinchu, Taiwan.

They were later measured at the University of Central Florida, Orlando FL, USA.

Three devices with the following makeup were used: Undoped poly-Si NW body with a rectangular cross section of 60nm x 18nm, channel lengths of 0.4, 1.0, and 2.0 mm, n+ polysilicon gate with $10^{21}$ cm$^{-3}$ doping, gate SiO$_2$ oxide thickness of 20nm, and S/D doping density of $5\times10^{20}$ cm$^{-3}$.
In weak inversion, $H_1$ and $H_2$ approximate the same value of $nv_{th}$.

$H_2$ is less noisy than $H_1$.

In strong inversion, $H_1$ and $H_2$ tend to be straight lines with slopes $1/(m+1)$ and $1/(m+2)$ respectively.

The values extracted from the straight line are $m = 2.1023$, and $V_{Ts} = 0.92$ V.
Knowing the values of $m$ and $V_{Ts}$ from the linear fit, we calculate $K$ by using:

$$K = \frac{I_{Ds}}{(V_G - V_{Ts})^m V_D}$$

$K$ looks fairly constant at a mean value of $K = 158.78 \text{ nA} / V^{(m+1)}$, for the chosen $V_G$ range.

As a confirmation, we present the measured transfer characteristic together with the model playback.
Phenomenological threshold voltage

Finally, the phenomenological threshold voltage $V_T$ is obtained as the value of $V_G$ where $H_{\text{weak}}$ intersects the linear extrapolation of the strong inversion region of $H_2 (H_{2S})$.

A value of $V_T = 1.63 \text{ V}$ is the result for this device.
4.3. Recent Derivative method for organic transistors [SI13]

For strong conduction:

\[ I_D = K (V_G - V_T)^m \]

Using LE method for \( I_D^{0.5} \), at an arbitrary value of gate bias \( V_{Gx} \):

\[ V_{T-LE} = V_{Gx} - \left[ \frac{\sqrt{I_D}}{d \sqrt{I_D}} \right]_{V_G=V_{Gx}} \]

The previous equation is evaluated using experimental data. Finally, \( V_T \) and \( m \) are extracted using the following equation:

\[ V_{T-LE} = \left( 1 - \frac{2}{m} \right) V_{Gx} - \frac{2}{m} V_T \]


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We observe that this derivative is too noisy: \( \frac{d\sqrt{I_D}}{dV_G} \)

\( V_{T-LE} \) is useless because of the high experimental noise.

\[
V_{T-LE} = V_{Gx} - \left[ \frac{\sqrt{I_D}}{d\sqrt{I_D}} \right] \frac{d\sqrt{I_D}}{dV_G} \bigg|_{V_G=V_{Gx}}
\]

It is not possible to see the expected straight line:

\[
V_{T-LE} = \left( 1 - \frac{2}{m} \right) V_{Gx} - \frac{2}{m} V_T
\]
5. $V_T$ extraction from small signal high frequency measurements

MOSFET’s model for high-frequency generally requires parameter extraction first in DC and then in high frequency.

Errors in the DC extraction procedure will produce errors in the high frequency parameters.

Álvarez-Botero et al [AL11] recently proposed to obtain all the parameters from the high frequency measurements.

5.1. Conductance-to-square-root-Conductance’s derivative-Ratio ($C_{srCdR}$) method

Kong et al proposed in 2001 [KO01] the following function:

$$C_{srCdR} \equiv \frac{g_{dsm}}{\sqrt{d g_{dsm} / d V_G}} = \beta^{1/2} \left( V_G - V_T \right)$$

where $g_{dsm}$ is the measured small signal conductance and

$$\beta \equiv \frac{W}{L} \mu Co$$

$C_{srCdR}$ is linear with $V_G$ for strong inversion and its extrapolation to $C_{srCdR}=0$ yields to $V_T$.


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This method (CsrCdR), developed in 2001, seems to be inspired in the previous Current-to-square-root-Transconductance Ratio (CsrTR) method, proposed in 1988 [JA88; GH88]:

$$CsrTR \equiv \frac{I_D}{\sqrt{dI_D/dV_G}} = s^{-1/2} \left( V_G - V_T \right)$$

We note that by replacing $I_D$ by $g_{dsm}$ in the previous equation (CsrTR) we obtain the definition of CsrCdR:

$$CsrCdR \equiv \frac{g_{dsm}}{\sqrt{dg_{dsm}/dV_G}} = \beta^{1/2} \left( V_G - V_T \right)$$


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5.2. Linear extrapolation of the intrinsic small-signal drain-source conductance (LESSC)

Álvarez-Botero et al [AL11] recently proposed to obtain all the parameters from the high frequency measurements. Then, the intrinsic small-signal conductance between source and drain \( g_{ch} \) at \( V_{ds} = 0 \) is:

\[
g_{ch} = \beta \left( V_G - V_T \right)
\]

\( g_{ch} \) is linear with \( V_G \) and its extrapolation to \( g_{ch} = 0 \) yields to \( V_T \).


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Conclusions

• We have presented, reviewed and critically compared several extraction methods used to determine the threshold voltage for crystalline and non-crystalline MOSFETs.

• The methods were compared under the same conditions by applying them to:

  (a) Measured characteristics of a crystalline MOSFET with state-of-the-art 65 nm channel length;

  (b) 2D simulations of a Double-Gate MOSFET; and

  (c) Measured characteristics of a polysilicon nanowire n-channel MOSFETs.

• The simulations have allowed to evaluate the methods under the presence of significant series resistance and several drain voltages.

• As a result of scrutinizing the methods, variations and improvements have been proposed.
END of presentation

Thank you for your attention

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Universidad Simón Bolívar
Caracas, Venezuela

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Idea Transition Method_piecewise-v22.mws 3-Aug2012

Idea Transition

Method_piecewise-v22.mws 3Aug2012

> restart: Digits:=20: withplots:
> ID:=piecewise( VG<VT, Ileak, VG=VT, K*(VG-VT)+Ileak )

    ID := \begin{cases} Ileak & VG < VT \\ K*(VG-VT)+Ileak & VT \leq VG \end{cases}

> inte:=int(ID,VG):

\begin{align*}
\text{inte} & := \begin{cases} Ileak VG & VG < VT \\ K\left(\frac{1}{2}VG^2-VT*VG\right)+Ileak VG+\frac{KVT^2}{2} & VT < VG \end{cases} \\
& - \begin{cases} Ileak & VG < VT \\ K*(VG-VT)+Ileak & VT \leq VG \end{cases}
\end{align*}

\[ G1 := VG \]

\[ G1 := VG \left(2\left(\frac{Ileak VG}{K\left(\frac{1}{2}VG^2-VT*VG\right)+Ileak VG+\frac{KVT^2}{2}}\right) \right) \\
& - \begin{cases} Ileak & VG < VT \\ K*(VG-VT)+Ileak & VT \leq VG \end{cases}
\]

\[ G1 \] := VG - 2*(K*(1/2*VG^2-VT*VG)/K*(VG-VT)+Ileak)

\[ G1 \] := VG - 2*(K*(1/2*VG^2-VT*VG)+Ileak*VG+1/2*K*VT^2)/(K*(VG-VT)+Ileak)

\[ G1 \] := VG - 2\left(\frac{K\left(\frac{1}{2}VG^2-VT*VG\right)+Ileak VG+\frac{KVT^2}{2}}{K*(VG-VT)+Ileak} \right)

\[ G1 \] := VG - \frac{K*(VG-VT)+Ileak}{K*(VG-VT)+Ileak}

> limit(G1strong, Ileak=0):

\[ VT \]

> ID:

\begin{align*}
\text{ID} & := \begin{cases} Ileak & VG < VT \\ K*(VG-VT)+Ileak & VT \leq VG \end{cases} \\
& K:=1; \quad VT:=.3; \quad \text{vth}:=0.0259; \quad \text{Ileak}:=1E-9;
\end{align*}

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Derivatives of semi empirical approximation for $I_D$ with Maple

```maple
Fit lateral Lambertiano de ID con degradation de movilidad-v6666.mws 21-jul-2012
> ID := (Io/(1+teta*VG))*W( (K1*(1+teta*VG))*exp( VG*b/n ));
> der1:=diff(ID, VG):  der2:=diff(der1, VG):  der3:=diff(der2, VG):
> der1ln:=diff( ln(ID), VG): der2ln:=diff(der1ln, VG): der3ln:=diff(der2ln, VG):
Caso numerico ya que no hay solucion analitica
> VT:=fsolve ( der3, VG=0.4..0.6):  VTln:=fsolve ( der3ln, VG=0.4..0.6): 
> IVT:=eval( ID, VG=VT):   IVTln:=eval( ID, VG=VTln):
> plot( {der1/1E-4}, VG=0.0..1.1):
> plot( {der2/5e-4}, VG=0.0..1.1):
> plot( {der3/4.5e-3}, VG=0.0..1.1):
> plot( {der1/1E-4,der2/5e-4,der3/4.5e-3}, VG=0.0..1.1):
> dvg:=0.01:     nmax:=110:
> for i from 0 by 1 to nmax do  vg[i]:=+0.0+i*dvg: id[i]:=eval(ID, VG=vg[i]):
deri1[i]:=eval(der1, VG=vg[i]):  deri2[i]:=eval(der2, VG=vg[i]):
deri3[i]:=eval(der3, VG=vg[i]):  deri2ln[i]:=eval(der2ln, VG=vg[i]): end do:
> for i from 0 by 1 to nmax do  lprint(vg[i],id[i],deri1[i],deri2[i],deri3[i]) end do:
```

"Exploring MOSFET threshold voltage..." EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.

>> restart:
> ID:=K*(VG-VT-(VD/2))*(VG-VT)**2: ID1:=(a+b*VG)/(1+c*VG+d*VG**2):
> a:=-b*(VT+VD/2): b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2): d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify(ID-ID1):
> restart:
> eq1:= a+b*(VT+VD/2): eq2:= -b+K*VD/(1-teta1*VT+teta2*VT**2):
> solve( {eq1,eq2,eq3,eq4}, {K,VT,teta1,teta2}):
> restart;
> K1 := 4*b^3/(4*d*a*b*VD-4*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2)/VD:
> K2:=b/((1+c*VT+d*VT**2)*VD):
> a:=-b*(VT+VD/2): b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2): d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify(K1-K2):
> restart;
> teta1a := 4*d*b^3/(4*d*a*b*VD-4*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2):
> teta1b := ( c+2*d*VT)/(1+c*VT+d*VT**2):
> a:=-b*(VT+VD/2): b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2): d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify( teta1a-teta1b):
> restart;
> teta2a := 4*d*b^3/(4*d*a*b*VD-4*c*b^2*VD+4*d*a^2+d*b^2*VD^2+4*b^2):
> teta2b := d/(1+c*VT+d*VT**2):
> a:=-b*(VT+VD/2): b:=K*VD/(1-teta1*VT+teta2*VT**2):
> c:=(teta1-2*teta2*VT)/(1-teta1*VT+teta2*VT**2): d:=teta2/(1-teta1*VT+teta2*VT**2):
> simplify( teta2a-teta2b):

"Exploring MOSFET threshold voltage..." EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
Using the “MOSFet” tool in nanohub: Structural Properties

MOSFET tool (v. 1.0padre)

Learn about Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as you explore the devices in this simulator.

Input values for the various parameters on the left and click “Simulate” at the top to run the simulation.
(Note: After the simulation has finished, 3D plots may still take some more time to load.)

Parameters:
- Structural Properties
  General properties of the materials used, such as physical dimensions and doping.
- Model
  Toggle simulation parameters to take certain physical phenomena into account, such as impact ionization, at the sacrifice of computation speed.
  Also define the effects the surroundings have on the device, including temperature.
- Voltage Sweep
  Define the effects the surroundings have on the device, including applied voltage.

MOSFET model notes:
- V_substrate, the voltage applied to the substrate is tied to the source and is always grounded. The user can vary the gate and drain voltages with respect to grounded.
Using the “MOSFet” tool in nanohub: Model

“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al.
Using the “MOSFet” tool in nanohub: Voltage Sweep

“Exploring MOSFET threshold voltage...” EDS DL, INAOE, Puebla, Mexico, Sept 2013, Ortiz-Conde et al. 73